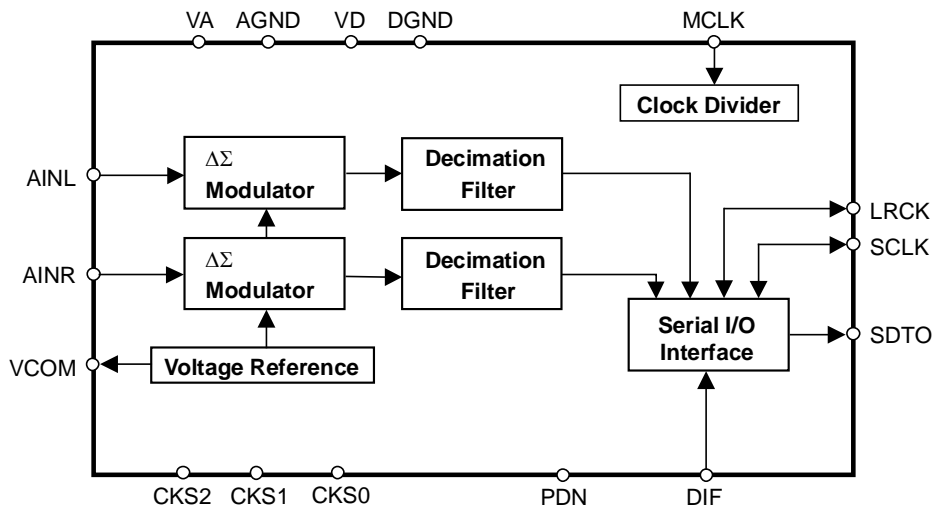
	<h1 style="margin: 0;">AK5359</h1> <h2 style="margin: 0;">24-Bit 192kHz <math>\Delta\Sigma</math> ADC</h2>
---	--

**GENERAL DESCRIPTION**

The AK5359 is a stereo A/D Converter with wide sampling rate of 8kHz ~ 216kHz and is suitable for consumer to professional audio system. The AK5359 achieves high accuracy and low cost by using Enhanced dual bit  $\Delta\Sigma$  techniques. The AK5359 requires no external components because the analog inputs are single-ended. The audio interface has two formats (MSB justified,  $I^2S$ ) and can correspond to various systems like DTV, DVR and AV Receiver.

**FEATURES**

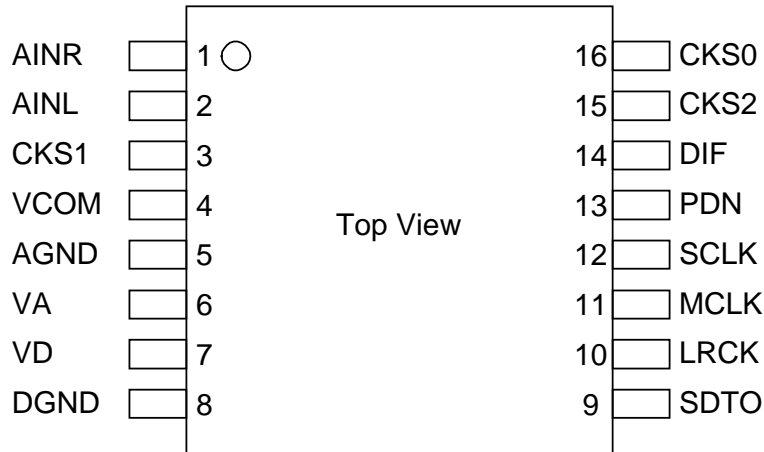
- Linear Phase Digital Anti-Alias Filtering
- Single-ended Input
- Digital HPF for DC-Offset cancel
- S/(N+D): 94dB
- DR: 102dB
- S/N: 102dB
- Sampling Rate Ranging from 8kHz to 216kHz
- Master Clock:
  - 256fs/384fs/512fs/768fs (8kHz ~ 54kHz)
  - 256fs/384fs (54kHz ~ 108kHz)
  - 256fs/384fs (108kHz ~ 216kHz)
- Input level: CMOS
- Master / Slave Mode
- Audio Interface: 24bit MSB justified /  $I^2S$  selectable
- Power Supply: 4.5 ~ 5.5V (Analog), 3.0 ~ 5.5V (Digital)
- Ta = -20 ~ 85°C (ET), -40 ~ 85°C (VT)
- Small 16pin TSSOP Package
- AK5357/58/81 Pin-compatible



■ Ordering Guide

AK5359ET	-20 ~ +85°C	16pin TSSOP (0.65mm pitch)
AK5359VT	-40 ~ +85°C	16pin TSSOP (0.65mm pitch)
AKD5359	Evaluation Board for AK5359	

■ Pin Layout



■ Compatibility with AK5357, AK5359 and AK5381

	AK5357	AK5358	AK5381	AK5359
fs	4kHz to 96kHz	8kHz to 96kHz	4kHz to 96kHz	8kHz to 216kHz
S/(N+D)	88dB	92dB	96dB	94dB
DR	102dB	102dB	106dB	102dB
VIH@TTL Level Mode	2.2V	2.2V	2.4V	Not Available
VA (Analog Supply)	2.7 to 5.5V	4.5 to 5.5V	4.5 to 5.5V	4.5 to 5.5V
VD (Digital Supply)	2.7 to 5.5V	2.7 to 5.5V	2.7 to 5.5V	3.0 to 5.5V
			3.0 to 5.5V @96kHz	
HPF Disable	Available	Not Available	Available	Available
Operating Temperature	ET: -20 ~ +85°C	ET: -20 ~ +85°C	ET: -20 ~ +85°C	ET: -20 ~ +85°C
	VT: -40 ~ +85°C		VT: -40 ~ +85°C	
			XT: -40 ~ +85°C	

PIN / FUNCTION			
No.	Pin Name	I/O	Function
1	AINR	I	Rch Analog Input Pin
2	AINL	I	Lch Analog Input Pin
3	CKS1	I	Mode Select 1 Pin
4	VCOM	O	Common Voltage Output Pin, VA/2 Bias voltage of ADC input.
5	AGND	-	Analog Ground Pin
6	VA	-	Analog Power Supply Pin, 4.5 ~ 5.5V
7	VD	-	Digital Power Supply Pin, 3.0 ~ 5.5V
8	DGND	-	Digital Ground Pin
9	SDTO	O	Audio Serial Data Output Pin “L” Output at Power-down mode.
10	LRCK	I/O	Output Channel Clock Pin “L” Output in Master Mode at Power-down mode.
11	MCLK	I	Master Clock Input Pin
12	SCLK	I/O	Audio Serial Data Clock Pin “L” Output in Master Mode at Power-down mode.
13	PDN	I	Power Down Mode & Reset Pin “H”: Power up, “L”: Power down & Reset The AK5359 must be reset once upon power-up.
14	DIF	I	Audio Interface Format Pin “H”: 24bit I <sup>2</sup> S Compatible, “L”: 24bit MSB justified
15	CKS2	I	Mode Select 2 Pin
16	CKS0	I	Mode Select 0 Pin

Note: All input pins except analog input pins (AINR, AINL) should not be left floating.

#### ■ Handling of Unused Pin

The unused input pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog	AINL	This pin should be open.
	AINR	This pin should be open.

<b>ABSOLUTE MAXIMUM RATINGS</b>
---------------------------------

(AGND, DGND=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog	VA	-0.3	6.0	V
	Digital	VD	-0.3	6.0	V
	$ AGND - DGND $ (Note 2)	$\Delta GND$	-	0.3	V
Input Current, Any Pin Except Supplies		IIN	-	$\pm 10$	mA
Analog Input Voltage (AINL, AINR, CKS1 pins)		VINA	-0.3	VA+0.3	V
Digital Input Voltage (Note 3)		VIND	-0.3	VD+0.3	V
Ambient Temperature (powered applied)	AK5359ET	Ta	-20	85	°C
	AK5359VT	Ta	-40	85	°C
Storage Temperature		Tstg	-65	150	°C

Note 1. All voltages with respect to ground.

Note 2. AGND and DGND must be connected to the same analog ground plane.

Note 3. PDN, DIF, MCLK, SCLK, LRCK, CKS0, CKS2 pins

WARNING: Operation at or beyond these limits may result in permanent damage to the device.  
Normal operation is not guaranteed at these extremes.

<b>RECOMMENDED OPERATING CONDITIONS</b>
---

(AGND, DGND=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies (Note 4)	Analog	VA	4.5	5.0	5.5	V
	Digital	VD	3.0	5.0	VA	V

Note 4. The power up sequence between VA and VD is not critical.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

**ANALOG CHARACTERISTICS**

(Ta=25°C; VA=VD=5.0V; AGND=DGND=0V; fs=48kHz; SCLK=64fs; Signal Frequency=1kHz; 24bit Data; Measurement frequency=20Hz ~ 20kHz at fs=48kHz, unless otherwise specified)

Parameter			min	typ	max	Units
<b>ADC Analog Input Characteristics:</b>						
Resolution					24	Bits
Input Voltage (Note 5)			2.7	3.0	3.3	Vpp
S/(N+D)	fs=48kHz BW=20kHz	-1dBFS	84	94		dB
		-60dBFS	-	39		dB
	fs=96kHz BW=40kHz	-1dBFS	82	92		dB
		-60dBFS	-	38		dB
	fs=192kHz BW=40kHz	-1dBFS	-	90		dB
		-60dBFS	-	38		dB
DR (-60dBFS, A-weighted)			94	102		dB
S/N (A-weighted)			94	102		dB
Input Resistance		fs=48kHz	13	20		kΩ
		fs=96kHz,192kHz	9	14		kΩ
Interchannel Isolation			90	110		dB
Interchannel Gain Mismatch				0.1	0.5	dB
Gain Drift				100	-	ppm/°C
Power Supply Rejection (Note 6)			-	50		dB
<b>Power Supplies</b>						
Power Supply Current						
Normal Operation (PDN pin = "H")						
VA				15	24	mA
VD (fs=48kHz)				4	6	mA
VD (fs=96kHz)				7	10	mA
VD (fs=192kHz)				10	16	mA
Power down mode (PDN pin = "L") (Note 7)						
VA+VD				10	100	μA

Note 5. This value is the full scale (0dB) of the input voltage. Input voltage is proportional to VA voltage.

$$V_{in} = 0.6 \times V_A \text{ (Vpp)}$$

Note 6. PSR is applied to VA and VD with 1kHz, 50mVpp.

Note 7. All digital input pins and CKS1 pin are held VD or DGND.

**FILTER CHARACTERISTICS (fs=48kHz)**

(Ta=Tmin ~ Tmax; VA=4.5 ~ 5.5V; VD=3.0 ~ 5.5V)

Parameter	Symbol	min	typ	max	Units
<b>ADC Digital Filter (Decimation LPF):</b>					
Passband (Note 8)	±0.1dB	PB	0	18.9	kHz
	-0.2dB		-	20.0	kHz
	-3.0dB		-	23.0	kHz
Stopband	SB	28			kHz
Passband Ripple	PR			±0.04	dB
Stopband Attenuation	SA	68			dB
Group Delay Distortion	ΔGD		0		μs
Group Delay (Note 9)	GD		16		1/fs
<b>ADC Digital Filter (HPF):</b>					
Frequency Response (Note 8)	-3dB	FR		1.0	Hz
	-0.1dB			6.5	Hz

**FILTER CHARACTERISTICS (fs=96kHz)**

(Ta=Tmin ~ Tmax ; VA=4.5 ~ 5.5V; VD=3.0 ~ 5.5V)

Parameter	Symbol	min	typ	max	Units
<b>ADC Digital Filter (Decimation LPF):</b>					
Passband (Note 8)	±0.1dB	PB	0	37.8	kHz
	-0.2dB		-	40.0	kHz
	-3.0dB		-	46.0	kHz
Stopband	SB	56			kHz
Passband Ripple	PR			±0.04	dB
Stopband Attenuation	SA	68			dB
Group Delay Distortion	ΔGD		0		μs
Group Delay (Note 9)	GD		16		1/fs
<b>ADC Digital Filter (HPF):</b>					
Frequency Response (Note 8)	-3dB	FR		2.0	Hz
	-0.1dB			13.0	Hz

**FILTER CHARACTERISTICS (fs=192kHz)**

(Ta=Tmin ~ Tmax ; VA=4.5 ~ 5.5V; VD=3.0 ~ 5.5V)

Parameter	Symbol	min	typ	max	Units
<b>ADC Digital Filter (Decimation LPF):</b>					
Passband (Note 8)	±0.1dB	PB	0	61.4	kHz
	-0.2dB		-	62.7	kHz
	-3.0dB		-	90.9	kHz
Stopband	SB	111			kHz
Passband Ripple	PR			±0.02	dB
Stopband Attenuation	SA	70			dB
Group Delay Distortion	ΔGD		0		μs
Group Delay (Note 9)	GD		16		1/fs
<b>ADC Digital Filter (HPF):</b>					
Frequency Response (Note 8)	-3dB	FR		4.0	Hz
	-0.1dB			26.0	Hz

Note 8. The passband and stopband frequencies scale with fs.

For example, PB=18.9kHz@±0.1dB is  $0.39375 \times fs$ .

Note 9. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the setting of 24bit data both channels to the ADC output register for ADC.

<b>DC CHARACTERISTICS</b>
---------------------------

(Ta=Tmin ~ Tmax ; VA=4.5 ~ 5.5V; VD=3.0 ~ 5.5V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	70%VD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%VD	V
High-Level Output Voltage (Iout=-1mA)	VOH	VD-0.5	-	-	V
Low-Level Output Voltage (Iout=1mA)	VOL	-	-	0.5	V
Input Leakage Current	Iin	-	-	±10	μA

<b>SWITCHING CHARACTERISTICS</b>
----------------------------------

(Ta=Tmin ~ Tmax ; VA=4.5 ~ 5.5V; VD=3.0 ~ 5.5V; CL=20pF)

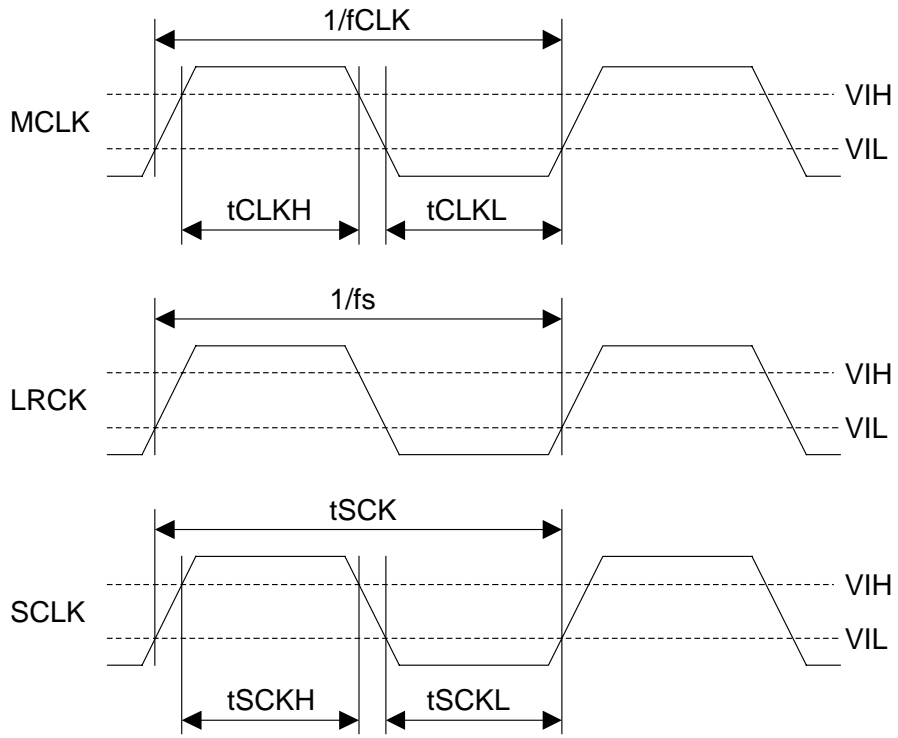
Parameter	Symbol	min	typ	max	Units
<b>Master Clock Timing</b>					
Frequency	fCLK	2.048		41.472	MHz
Pulse Width Low	tCLKL	0.4/fCLK			ns
Pulse Width High	tCLKH	0.4/fCLK			ns
<b>LRCK Frequency</b>					
	fs	8		216	kHz
Duty Cycle	Slave mode	45		55	%
	Master mode		50		%
<b>Audio Interface Timing</b>					
<b>Slave mode</b>					
SCLK Period	tSCK	72			ns
SCLK Pulse Width Low	tSCKL	33			ns
Pulse Width High	tSCKH	33			ns
LRCK Edge to SCLK “↑” (Note 10)	tLRSH	20			ns
SCLK “↑” to LRCK Edge (Note 10)	tSHLR	20			ns
LRCK to SDTO (MSB) (Except I <sup>2</sup> S mode)	tLRS			25	ns
SCLK “↓” to SDTO	tSSD			25	ns
<b>Master mode</b>					
SCLK Frequency	fSCK		64fs		Hz
SCLK Duty	dSCK		50		%
SCLK “↓” to LRCK	tMSLR	-20		20	ns
SCLK “↓” to SDTO	tSSD	-20		20	ns
<b>Reset Timing</b>					
PDN Pulse Width (Note 11)	tPD	150			ns
PDN “↑” to SDTO valid at Slave Mode (Note 12)	tPDV		4132		1/fs
PDN “↑” to SDTO valid at Master Mode (Note 12)	tPDV		4129		1/fs

Note 10. SCLK rising edge must not occur at the same time as LRCK edge.

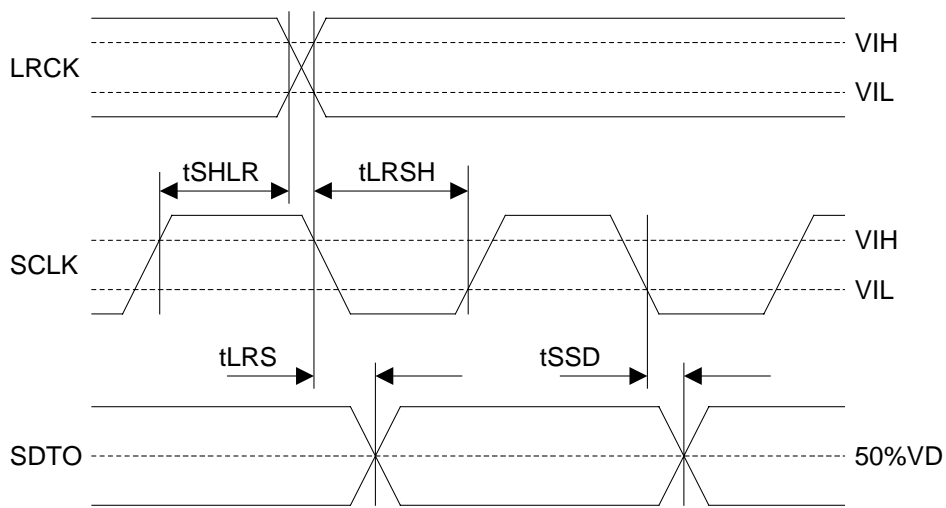
Note 11. The AK5359 can be reset by bringing the PDN pin = “L”.

Note 12. This cycle is the number of LRCK rising edges from the PDN pin = “H”.

■ Timing Diagram

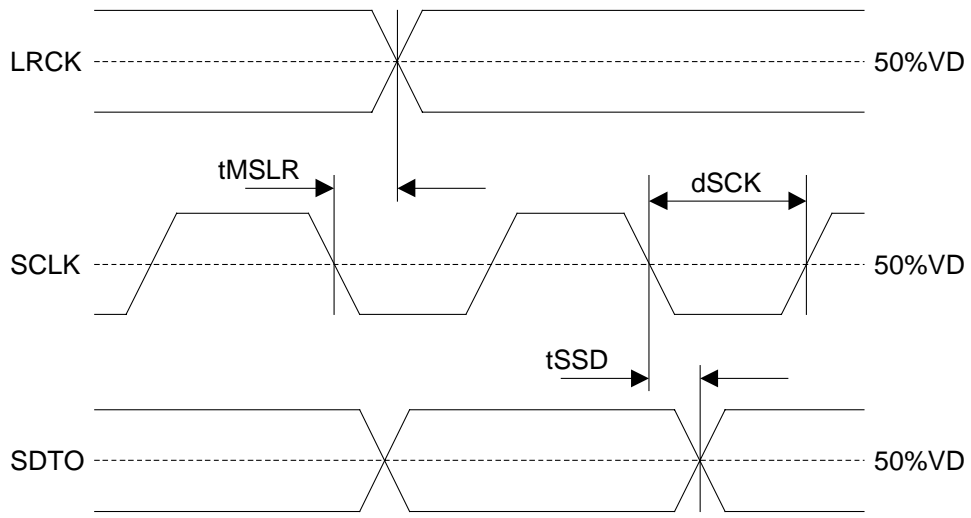


Clock Timing

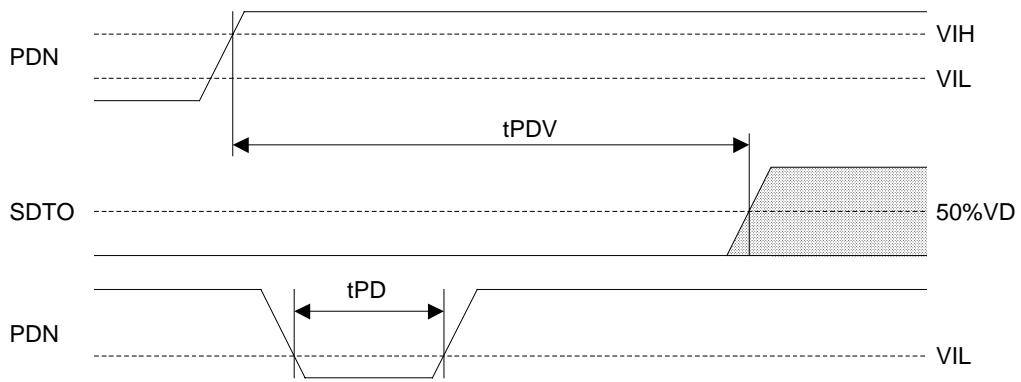


Audio Interface Timing (Slave mode)





Audio Interface Timing (Master mode)



Power Down & Reset Timing

<b>OPERATION OVERVIEW</b>
---------------------------

### ■ System Clock

MCLK, SCLK and LRCK (fs) clocks are required in slave mode. The LRCK clock input must be synchronized with MCLK, however the phase is not critical. Table 1 shows the relationship of typical sampling frequency and the system clock frequency. MCLK frequency, SCLK frequency, HPF (ON or OFF) and master/slave are selected by CKS2-0 pins as shown in Table 2.

All external clocks (MCLK, SCLK and LRCK) must be present unless PDN pin = "L". If these clocks are not provided, the AK5359 may draw excess current due to its use of internal dynamically refreshed logic. If the external clocks are not present, place the AK5359 in power-down mode (PDN pin = "L"). In master mode, the master clock (MCLK) must be provided unless PDN pin = "L".

fs	MCLK					
	128fs	192fs	256fs	384fs	512fs	768fs
32kHz	N/A	N/A	8.192MHz	12.288MHz	16.384MHz	24.576MHz
44.1kHz	N/A	N/A	11.2896MHz	16.9344MHz	22.5792MHz	33.8688MHz
48kHz	N/A	N/A	12.288MHz	18.432MHz	24.576MHz	36.864MHz
96kHz	N/A	N/A	24.576MHz	36.864MHz	N/A	N/A
192kHz	24.576MHz	36.864MHz	N/A	N/A	N/A	N/A

Table 1. System Clock Example

CKS2	CKS1	CKS0	HPF	Master/Slave	MCLK	SCLK
L	L	L	ON	Slave	128/192fs (108k<fs≤216k) 256/384fs (8k≤fs≤108k) 512/768fs (8k≤fs≤54k)	≥ 48fs or 32fs
L	L	H	OFF	Slave	128/192fs (108k<fs≤216k) 256/384fs (8k≤fs≤108k) 512/768fs (8k≤fs≤54k)	≥ 48fs or 32fs
L	H	L	ON	Master	256fs (8k≤fs≤108k)	64fs
L	H	H	ON	Master	512fs (8k≤fs≤54k)	64fs
H	L	L	ON	Master	128fs (108k<fs≤216k)	64fs
H	L	H	ON	Master	192fs (108k<fs≤216k)	64fs
H	H	L	ON	Master	384fs (8k≤fs≤108k)	64fs
H	H	H	ON	Master	768fs (8k≤fs≤54k)	64fs

Table 2. Mode Select

Note: SDTO outputs 16bit data at SCLK=32fs.

### ■ Audio Interface Format

Two kinds of data formats can be chosen with the DIF pin (Table 3). In both modes, the serial data is in MSB first, 2's complement format. The SDTO is clocked out on the falling edge of SCLK. The audio interface supports both master and slave modes. In master mode, SCLK and LRCK are output with the SCLK frequency fixed to 64fs and the LRCK frequency fixed to 1fs.

Mode	DIF pin	SDTO	LRCK	SCLK	Figure
0	L	24bit, MSB justified	H/L	≥ 48fs or 32fs	Figure 1
1	H	24bit, I <sup>2</sup> S Compatible	L/H	≥ 48fs or 32fs	Figure 2

Table 3. Audio Interface Format

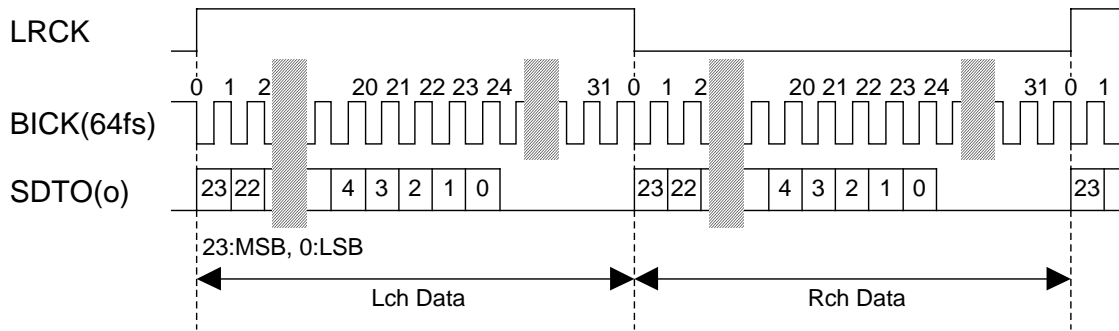


Figure 1. Mode 0 Timing

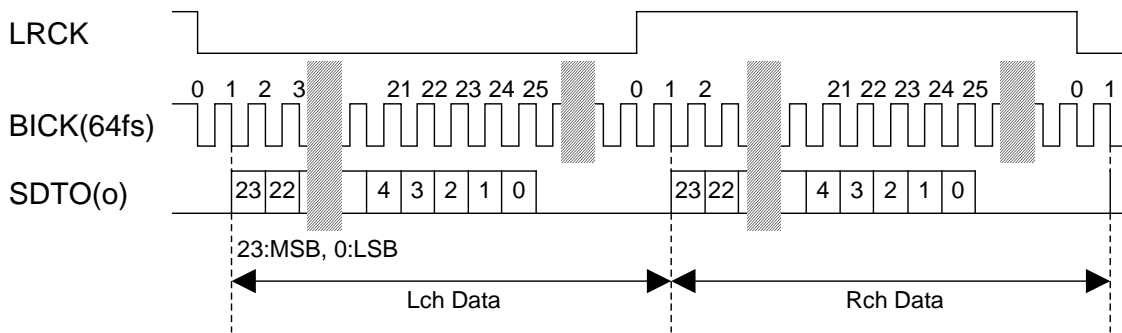


Figure 2. Mode 1 Timing

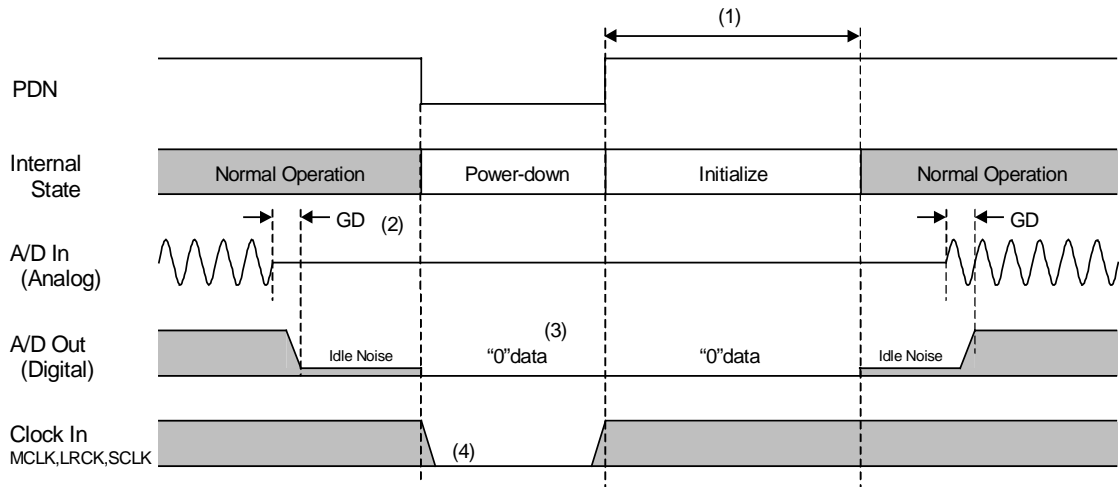
■ Digital High Pass Filter

The ADC has a digital high pass filter for DC offset cancellation. The cut-off frequency of the HPF is 1.0Hz (@fs=48kHz) and scales with sampling rate (fs).

HPF is controlled by CKS2-0 pins (Table 2). If HPF setting (ON/OFF) is changed at operating, click noise occurs by changing DC offset. It is recommended that HPF setting is changed at PDN pin = "L".

■ Power down

The AK5359 is placed in the power-down mode by bringing PDN pin “L” and the digital filter is also reset at the same time. This reset should always be done after power-up. In the power-down mode, the VCOM are AGND level. An analog initialization cycle starts after exiting the power-down mode. Therefore, the output data SDTO becomes available after 4129 cycles of LRCK clock in master mode or 4132 cycles of LRCK clock in slave mode. During initialization, the ADC digital data outputs of both channels are forced to a 2’s complement “0”. The ADC outputs settle in the data corresponding to the input signals after the end of initialization (Settling approximately takes the group delay time).



Notes:

- (1) 4132/fs in slave mode and 4129/fs in master mode.
- (2) Digital output corresponding to analog input has the group delay (GD).
- (3) A/D outputs “0” data at the power-down state.
- (4) When the external clocks (MCLK, SCLK and LRCK) are stopped, the AK5359 should be in the power-down state.

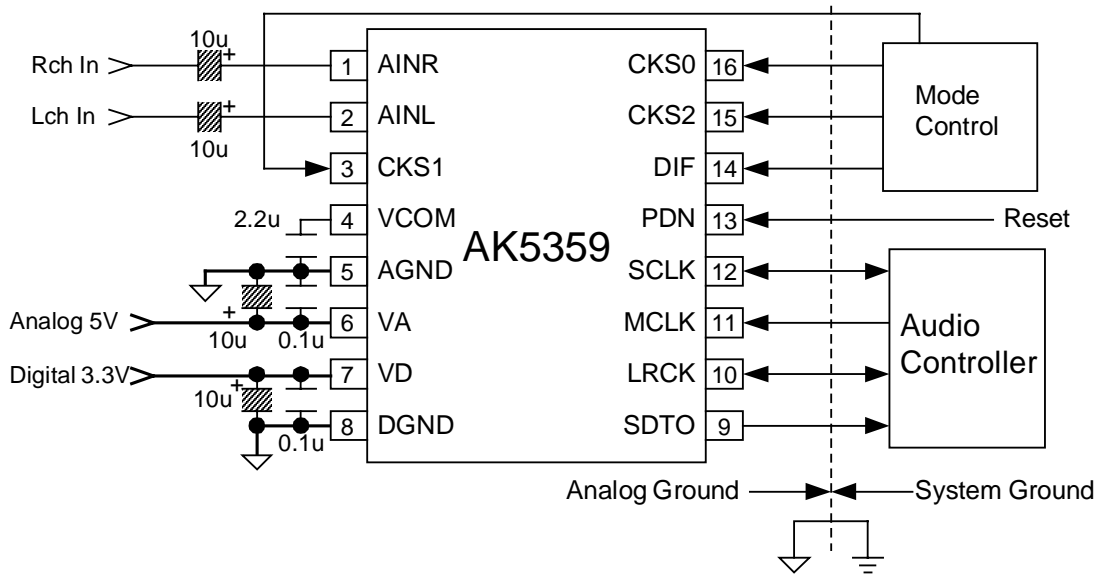
Figure 3. Power-down/up sequence example

■ System Reset

The AK5359 should be reset once by bringing PDN pin “L” after power-up. In slave mode, the internal timing starts clocking by the rising edge (falling edge at mode 1) of LRCK after exiting from reset and power down state by MCLK. The AK5359 is power down state until LRCK is input. In master mode, the internal timing starts when MCLK is input.

**SYSTEM DESIGN**

Figure 4 shows the system connection diagram. An evaluation board is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.



- Note:
- AGND and DGND of the AK5359 should be distributed separately from the ground of external digital devices (MPU, DSP etc.).
  - All digital input pins should not be left floating.
  - The CKS1 pin should be connected to VA or AGND.

Figure 4. Typical Connection Diagram

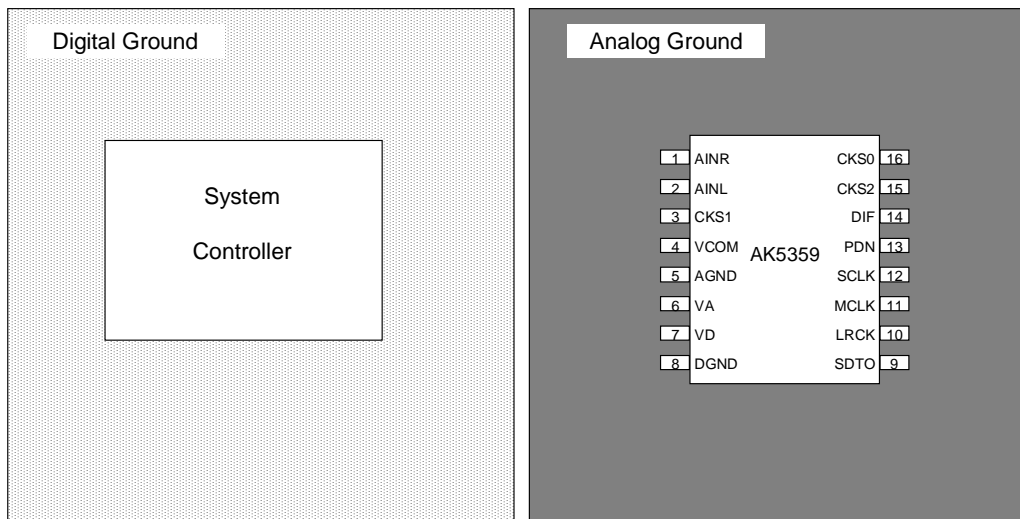


Figure 5. Ground Layout

- Note:
- AGND and DGND must be connected to the same analog ground plane.

## 1. Grounding and Power Supply Decoupling

The AK5359 requires careful attention to power supply and grounding arrangements. Alternatively if VA and VD are supplied separately, the power up sequence is not critical. **AGND and DGND of the AK5359 must be connected to analog ground plane.** System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK5359 as possible, with the small value ceramic capacitor being the nearest.

## 2. Voltage Reference

The voltage input to VA sets the analog input range. VCOM are 50% VA and normally connected to AGND with a 0.1 $\mu$ F ceramic capacitor. A capacitor 2.2 $\mu$ F is attached to VCOM pin. No load current may be drawn from these pins. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK5359.

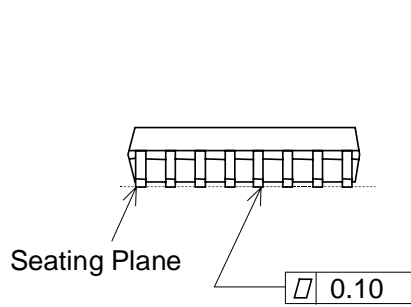
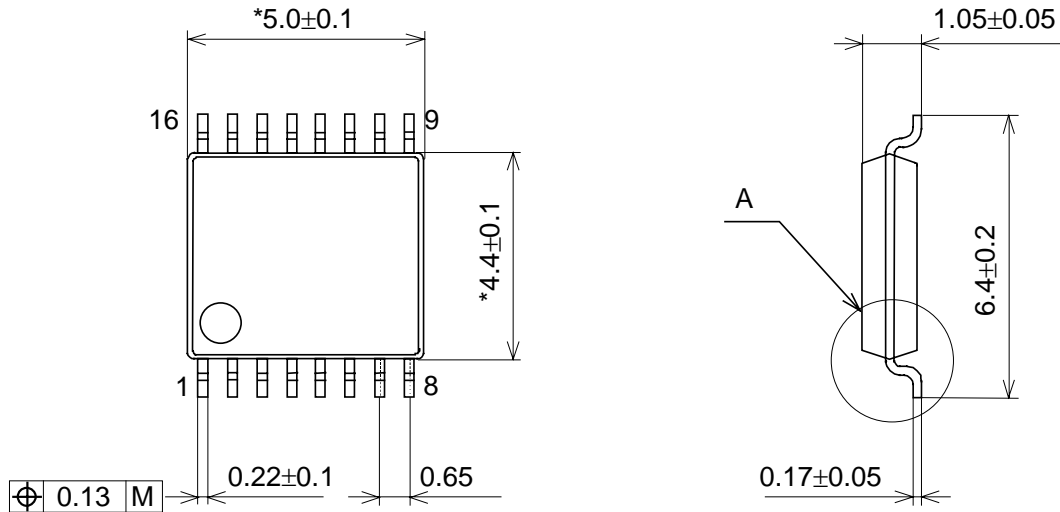
## 3. Analog Inputs

The ADC inputs are single-ended and internally biased to the common voltage (50% VA) with 20k $\Omega$  (typ@fs=48kHz) resistance. The input signal range scales with the supply voltage and nominally 0.6xVA Vpp (typ). The ADC output data format is 2's complement. The internal HPF removes the DC offset.

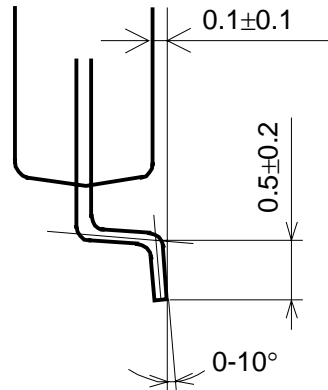
The AK5359 samples the analog inputs at 64fs (@fs=48kHz, 96kHz) or 32fs(@192kHz). The digital filter rejects noise above the stop band except for multiples of 64fs or 32fs. The AK5359 includes an anti-aliasing filter (RC filter) to attenuate a noise around 64fs or 32fs.

**PACKAGE**

**16pin TSSOP (Unit: mm)**



**Detail A**

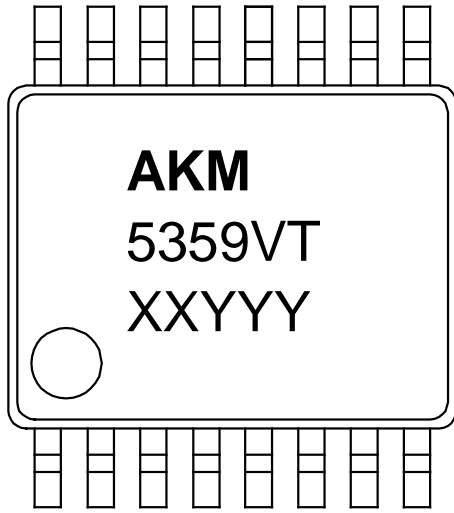


NOTE: Dimension "\*" does not include mold flash.

**Material & Lead finish**

- Package molding compound: Epoxy
- Lead frame material: Cu
- Lead frame surface treatment: Solder (Pb free) plate

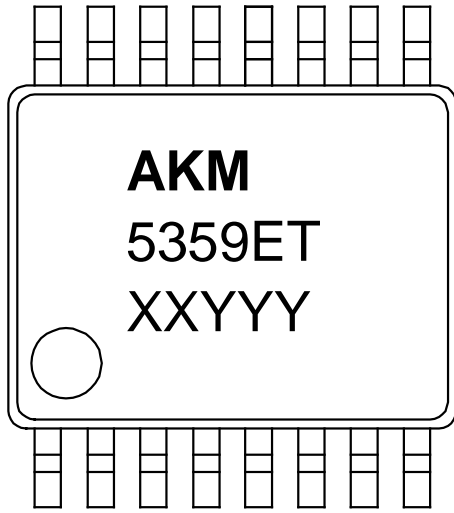
**MARKING (AK5359VT)**



- 1) Pin #1 indication
- 2) Date Code: XXYYYY (5 digits)  
    XX: Lot#  
    YYY: Date Code
- 3) Marketing Code: 5359VT



**MARKING (AK5359ET)**



- 1) Pin #1 indication
- 2) Date Code: XXYYYY (5 digits)
  - XX: Lot#
  - YYY: Date Code
- 3) Marketing Code: 5359ET

<b>Revision History</b>
-------------------------

Date (YY/MM/DD)	Revision	Reason	Page	Contents
05/09/30	00	First Edition		

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  - b. A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
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