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AK4499

Premium Switched Resistor 4ch DAC

1. General Description

The AK4499 is a 32-bit 4ch Switched Resistor DAC which adopts newly developed technology, achieving the industry's leading level low distortion and low noise characteristics. It corresponds to a 768kHz PCM input and an DSD512 input at maximum, suitable for playback of high resolution audio sources that are becoming widespread in Network Audio and USB-DACs Audio systems. In addition, it is capable of supporting a wide range of signals and achieving low out-of-band noise. The AK4499 has six types of 32-bit digital filters, realizing simple and flexible sound reproduction in wide range of applications.

2. Features

- 4-ch Switched Resistor DAC
- THD+N: -124 dB
- Dynamic Range, S/N: 140 dB (Mono), 137 dB (Stereo), 134 dB (4ch)
- 128x Over Sampling
- Sampling Rate: 8 kHz ~ 768 kHz
- 32-bit 8x Digital Filter
  - Short Delay Sharp Roll-off, GD = 6.0/fs
  - Short Delay Slow Roll-off, GD = 5.0/fs
  - Sharp Roll-off
  - Slow Roll-off
  - Super Slow Roll-off
  - Low Dispersion Short Delay Filter
- DSD64, DSD128, DSD256, DSD512 Input Support
  - Filter1 (fc = 37 kHz, DSD64 mode)
  - Filter2 (fc = 65 kHz, DSD64 mode)
- Digital De-emphasis for 32, 44.1 and 48kHz sampling
- Soft Mute
- Digital Attenuator (0 dB ~ -127 dB, 0.5 dB step + mute)
- Mono Mode
- External Digital Filter Interface (EXDF Mode)
- PCM/DSD, EXDF/DSD Mode Automatic Mode Switching Function
- Audio I/F Format
  - MSB Justified
  - LSB Justified
  - I^2S
  - DSD
  - TDM
- Daisy Chain
- Master Clock
  - fs = 8 kHz ~ 32 kHz: 256fs, 384fs, 512fs, 768fs, 1152fs
  - fs = 32 kHz ~ 54 kHz: 256fs, 384fs, 512fs, 768fs
  - fs = 54 kHz ~ 108 kHz: 256fs, 384fs
  - fs = 108 kHz ~ 216 kHz: 128fs, 192fs
  - fs = 384 kHz : 32fs, 48fs, 64fs, 96fs
  - fs = 768 kHz : 16fs, 32fs, 48fs, 64fs
- Register Control Mode with 3-wire Serial or I^2C interface

- Pin Control Mode
- Power Supply:
  Internal LDO (LDOE pin = “H”); TVDD = 3.0 ~ 3.6 V, AVDD = 4.75 ~ 5.25 V,
  VDDL1/R1/L2/R2 = 4.75 ~ 5.25 V
  External Supply (LDOE pin = “L”); TVDD = 1.7 ~ 3.6 V, DVDD = 1.7 ~ 1.98 V,
  AVDD = 4.75 ~ 5.25 V, VDDL1/R1/L2/R2 = 4.75 ~ 5.25 V
- Operational Temperature: -40 ~ 85 °C
- Digital Input Level: CMOS
- Package: 128-pin HTQFP

3. Block Diagram and Functions

3.1. Block Diagram

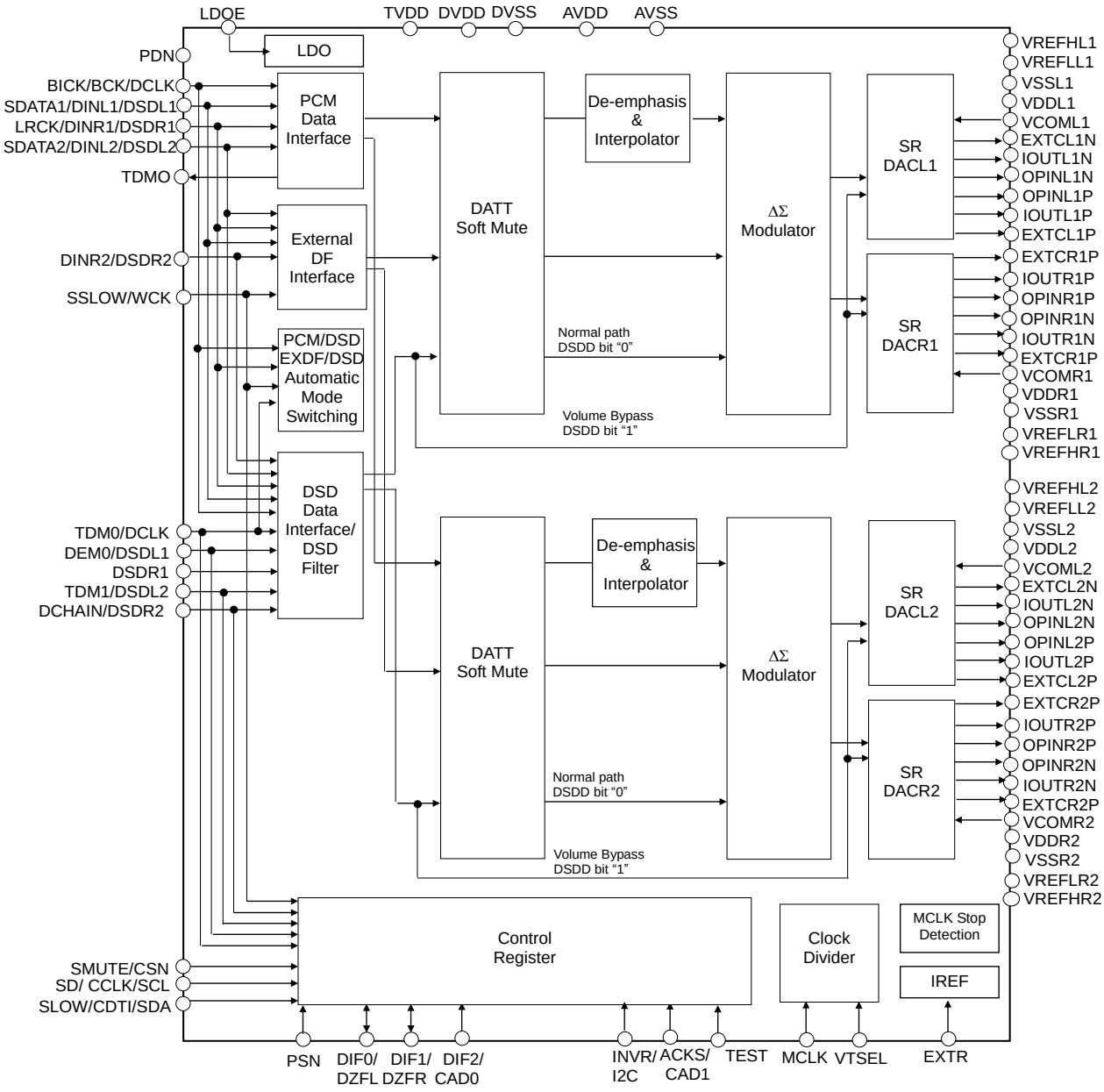


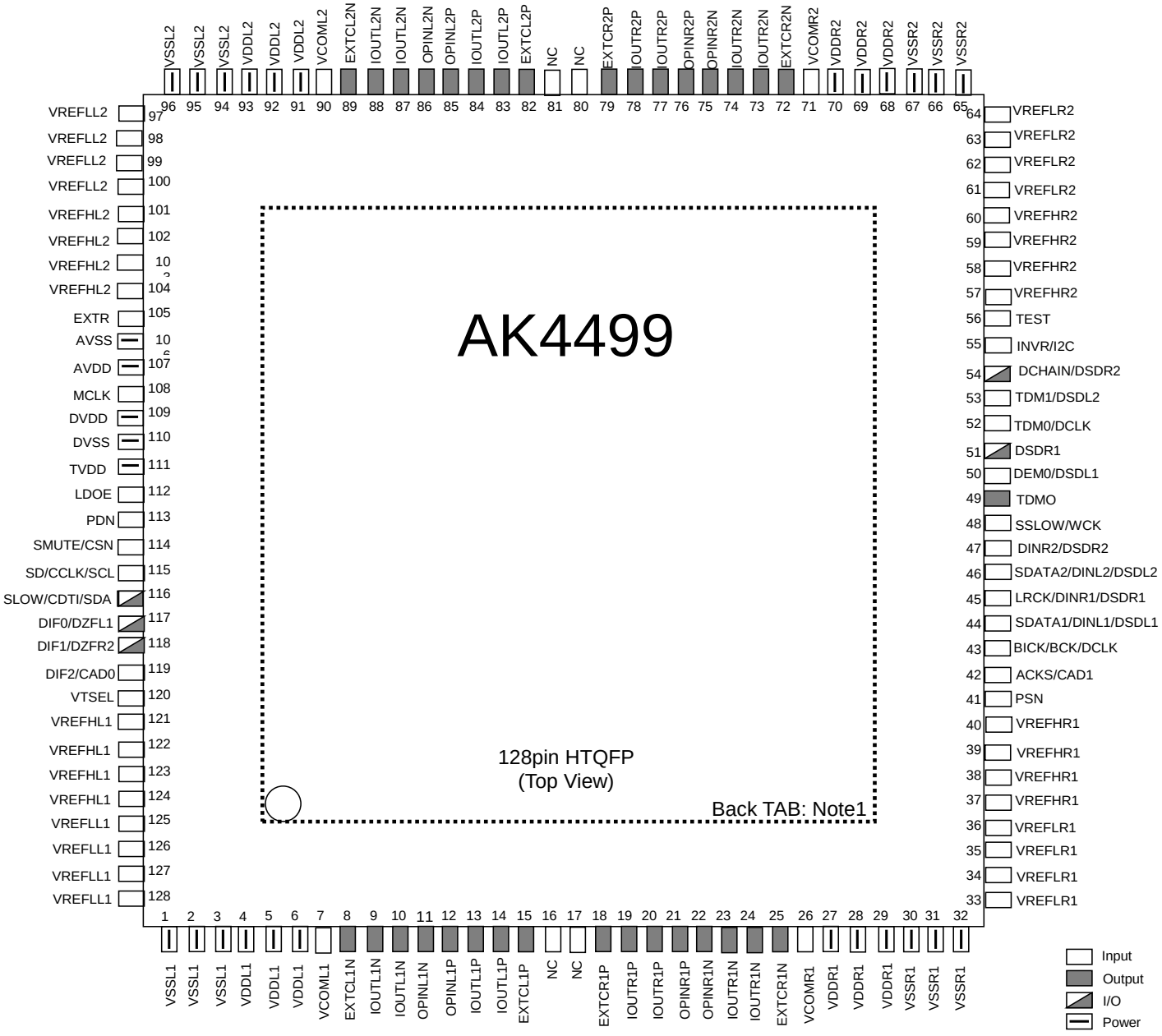
Figure 1. AK4499 Block Diagram

3.2. Functions

Block	Function
PCM Data Interface	Execute serial/parallel conversion of SDATA1/2 input data by synchronizing with LRCK and BICK, and generate TDM output data.
External DF Interface	Receive external digital filter outputs. Execute serial/parallel conversion of DINL1/2 and DINR1/2 input data by synchronizing with BICK.
DSD Data Interface	1-bit data that is input from DSDL1/2 and DSDR1/2 pins is received by synchronizing with DCLK.
DSD Filter	FIR filter that reduces high frequency noise of DSD input data
DATT, Soft Mute	Apply DATT and Soft Mute process to input data.
De-emphasis & Interpolator	A digital filter that applies De-emphasis process to input data and executes over sampling.
ΔΣ Modulator	Output multi-bit data to SR DAC. This block consists of a third-order digital delta-sigma modulator.
SR DAC	Convert multi bit output of ΔΣ Modulator into analog signal. This block consists of a switched resistor DAC.
Control Register	Keep register settings for each mode. Control registers are accessed in 3-wire (CSN, CCLK, CDTI) or I2C-Bus (SCL, SDA) control mode.
Clock Divider	Divide Master Clock In PCM mode, master clock is divided automatically by fs rate auto detection function. In DSD mode, the master clock frequency is set by DCKS bit.
MCLK Stop Detection	Detects when the master clock input is absent.
IREF	Generate reference current from the reference voltage generated internally, using an external resistor.
LDO	Generate power for internal digital circuit (1.8V typ.).

4. Pin Configurations and Functions

4.1. Pin Configurations



Note 1: The exposed pad on the bottom surface of the package must be connected to ground (AVSS).

4.2. Functions

No.	Pin Name	I/O	Function	Power Down State
1-3	VSSL1	-	L1ch Analog Ground pin.	-
4-6	VDDL1	-	L1ch Analog Power Supply pin.	-
7	VCOML1	I	L1ch VCOM pin. VCOML1 is connected to the midpoint of resistors between VREFHL1 and VREFL1.	Hi-Z
8	EXTCL1N	O	External Capacitor connection pin. This pin should be connected to 1 μF to VSSL1.	Pull-down to VSSL1 (250 kΩ, typ)
9,10	IOUTL1N	O	Current Output pin (L1ch Negative Signal).	Connected to OPINL1N (64 Ω, typ)
11	OPINL1N	O	Common Voltage Input pin (L1ch Negative Signal).	Connected to IOUTL1N (64 Ω, typ)
12	OPINL1P	O	Common Voltage Input pin (L1ch Positive Signal).	Connected to IOUTL1P (64 Ω, typ)
13,14	IOUTL1P	O	Current Output pin (L1ch Positive Signal).	Connected to OPINL1P (64 Ω, typ)
15	EXTCL1P	O	External Capacitor connection pin. This pin should be connected to 1 μF to VSSL1.	Pull-down to VSSL1 (250 kΩ, typ)
16,17	NC	-	No internal bonding. Connect to AVSS.	-
18	EXTCR1P	O	External Capacitor connection pin. This pin should be connected to 1 μF to VSSR1.	Pull-down to VSSR1 (250 kΩ, typ)
19,20	IOUTR1P	O	Current Output pin (R1ch positive signal).	Connected to OPINR1P (64 Ω, typ)
21	OPINR1P	O	Common Voltage input pin (R1ch positive signal).	Connected to IOUTR1P (64 Ω, typ)
22	OPINR1N	O	Common Voltage input pin (R1ch negative signal).	Connected to IOUTR1N (64 Ω, typ)
23,24	IOUTR1N	O	Current Output pin (R1ch negative signal).	Connected to OPINR1N (64 Ω, typ)
25	EXTCR1N	O	External Capacitor connection pin. This pin should be connected to 1 μF to VSSR1.	Pull-down to VSSR1 (250 kΩ, typ)
26	VCOMR1	I	R1ch VCOM pin. VCOMR1 is connected to the midpoint of resistors between VREFHR1 and VREFLR1.	Hi-Z
27-29	VDDR1	-	R1ch Analog Power Supply pin.	-
30-32	VSSR1	-	R1ch Analog Ground pin.	-
33-36	VREFLR1	I	R1ch Low Level Reference Voltage Input pin.	Hi-Z
37-40	VREFHR1	I	R1ch High Level Reference Voltage Input pin.	Hi-Z
41	PSN	I	Control Mode Select pin (Internal pull-up pin) "L": Register Control mode "H": Pin Control mode	Pull-Up to TVDD (100 kΩ, typ)

No.	Pin Name	I/O	Function	Power Down State
42	ACKS	I	Clock Setting Mode Select pin in Pin Control mode “L”: Fixed Speed mode “H”: Auto Setting mode	Hi-Z
	CAD1	I	Chip Address 1 pin in Register Control mode	
43	BICK	I	Audio Serial Data Clock pin in PCM mode	Hi-Z
	BCK	I	Audio Serial Data Clock pin in EXDF mode	
	DCLK	I	DSD Clock Pin in DSD mode (@DSDPATH bit = ”1”)	
44	SDATA1	I	Audio Serial Data Input pin in PCM mode	Hi-Z
	DINL1	I	Audio Serial Data Input pin in EXDF mode	
	DSDL1	I	Audio Serial Data Input pin in DSD mode (@DSDPATH bit = ”1”)	
45	LRCK	I	Input Channel Clock pin in PCM mode	Hi-Z
	DINR1	I	Audio Serial Data Input pin in EXDF mode	
	DSDR1	I	Audio Serial Data Input pin in DSD mode (@DSDPATH bit = ”1”)	
46	SDATA2	I	Audio Serial Data Input pin in PCM mode	Hi-Z
	DINL2	I	Audio Serial Data Input pin in EXDF mode	
	DSDL2	I	Audio Serial Data Input pin in DSD mode (@DSDPATH bit = ”1”)	
47	DINR2	I	Audio Serial Data Input pin in EXDF mode	Hi-Z
	DSDR2	I	Audio Serial Data Input pin in DSD mode (@DSDPATH bit = ”1”)	
48	SSLOW	I	Digital Filter Select pin in Pin Control mode	Hi-Z
	WCK	I	Word Clock input pin in EXDF mode	
49	TDMO	O	Audio Serial Data Output pin in Daisy Chain mode (Internal pull-down pin)	Pull-down to DVSS (100 kΩ, typ)
50	DEM0	I	De-emphasis Enable pin in Pin Control mode	Hi-Z
	DSDL1	I	Audio Serial Data Input pin in DSD mode (@DSDPATH bit = ”0”)	
51	DSDR1	I	Audio Serial Data Input pin in DSD mode (@DSDPATH bit = ”0”)	Hi-Z
52	TDM0	I	TDM Mode select 0 pin in Pin control mode.	Hi-Z
	DCLK	I	DSD Clock pin in DSD mode (@DSDPATH bit =”0”)	
53	TDM1	I	TDM Mode select 1 pin in Pin control mode.	Hi-Z
	DSDL2		Audio Serial Data Input pin in DSD mode (@DSDPATH bit = ”0”)	
54	DCHAIN	I	Daisy Chain Mode Select pin in Pin Control mode.	Hi-Z
	DSDR2	I	Audio Serial Data Input Pin in DSD mode (@DSDPATH bit = ”0”)	
55	INVR	I	R1/2ch Signal Invert pin in Pin Control mode	Hi-Z
	I2C	I	Serial Control Interface Select pin in Register Control mode. “L”: 3-wire serial control interface. “H”: I^2C Bus serial control interface.	
56	TEST	I	Connect to DVSS (Internal pull-down pin)	Pull-down to DVSS (100 kΩ, typ)

No.	Pin Name	I/O	Function	Power Down State
57-60	VREFHR2	I	R2ch High Level Reference Voltage Input pin.	Hi-Z
61-64	VREFLR2	I	R2ch Low Level Reference Voltage Input pin.	Hi-Z
65-67	VSSR2	-	R2ch Analog Ground pin.	-
68-70	VDDR2	-	R2ch Analog Power Supply pin.	-
71	VCOMR2	I	R2ch VCOM pin. VCOMR2 is connected to the midpoint of resistors between VREFHR2 and VREFLR2.	Hi-Z
72	EXTCR2N	O	External Capacitor Connection pin. This pin should be connected to 1 µF to VSSR2.	Pull-down to VSSR2 (250 kΩ, typ)
73,74	IOUTR2N	O	Current Output pin (R2ch negative signal).	Connected to OPINR2N (64 Ω, typ)
75	OPINR2N	O	Common Voltage Input pin (R2ch negative signal).	Connected to IOUTR2N (64 Ω, typ)
76	OPINR2P	O	Common Voltage Input pin (R2ch positive signal).	Connected to IOUTR2P (64 Ω, typ)
77,78	IOUTR2P	O	Current Output pin (R2ch positive signal).	Connected to OPINR2P (64 Ω, typ)
79	EXTCR2P	O	External Capacitor connection pin. This pin should be connected to 1 µF to VSSR2.	Pull-down to VSSR2 (250 kΩ, typ)
80,81	NC	-	No internal bonding. Connect to AVSS.	-
82	EXTCL2P	O	External Capacitor connection pin. This pin should be connected to 1 µF to VSSL2.	Pull-down to VSSL2 (250 kΩ, typ)
83,84	IOUTL2P	O	Current Output pin (L2ch positive signal).	Connected to OPINL2P (64 Ω, typ)
85	OPINL2P	O	Common Voltage Input pin (L2ch positive signal).	Connected to IOUTL2P (64 Ω, typ)
86	OPINL2N	O	Common Voltage Input pin (L2ch negative signal).	Connected to IOUTL2N (64 Ω, typ)
87,88	IOUTL2N	O	Current Output pin (L2ch negative signal).	Connected to OPINL2N (64 Ω, typ)
89	EXTCL2N	O	External Capacitor connection pin. This pin should be connected to 1 µF to VSSL2.	Pull-down to VSSL2 (250 kΩ, typ)
90	VCOML2	I	L2ch VCOM pin. VCOML2 is connected to the midpoint of resistors between VREFHL2 and VREFLL2.	Hi-Z
91-93	VDDL2	-	L2ch Analog Power Supply pin.	-
94-96	VSSL2	-	L2ch Analog Ground pin.	-
97-100	VREFLL2	I	L2ch Low Level Reference Voltage Input pin.	Hi-Z
101-104	VREFHL2	I	L2ch High Level Reference Voltage Input pin.	Hi-Z
105	EXTR	I	External Resistor connection pin. This pin should be connected to 33 kΩ (±1 %) to AVSS.	Hi-Z
106	AVSS	-	Analog Ground pin	-
107	AVDD	-	Clock Interface Power Supply Pin, 4.75 ~ 5.25 V	-

No.	Pin Name	I/O	Function	Power Down State
108	MCLK	I	Master Clock Input pin	Hi-Z
109	DVDD	O	(LDOE pin = "H") LDO Output pin. This pin should be connected to DVSS with 1.0 μF. This pin is prohibited to connect to other devices.	DVSS
		-	(LDOE pin = "L") 1.8 V Digital Power Supply pin	-
110	DVSS	-	Digital Ground pin	-
111	TVDD	-	Digital Power Supply pin, 3.0 V~3.6 V	-
112	LDOE	I	Internal LDO Enable pin. "L": Disable, "H": Enable	Hi-Z
113	PDN	I	Power-Up, Power-Down pin When at "L", the AK4499 is in Power-Down mode. The AK4499 must always be in Power-Down mode upon supply power on.	Hi-Z (PDN = "L")
114	SMUTE	I	When this pin is changed to "H", Soft Mute cycle is initiated. When returning to "L", Soft Mute releases.	Hi-Z
	CSN	I	Chip Select pin in 3-wire serial Register Control mode	
115	SD	I	Digital Filter Select pin in Pin Control mode	Hi-Z
	CCLK	I	Control Data Clock pin in 3-wire serial Register Control mode	
	SCL	I	Control Data Clock Input pin in I^2C Bus Register Control mode	
116	SLOW	I	Digital Filter Select pin in Pin Control mode	Hi-Z
	CDTI	I	Control Data Input pin in 3-wire serial Register Control mode	
	SDA	I/O	Control Data Input pin in I^2C Bus Register Control mode	
117	DIF0	I	Digital Input Format 0 pin in Pin Control mode	Pull-down to DVSS (100 kΩ, typ)
	DZFL	O	Lch Zero Input Detect pin in Register Control mode (Internal pull-down pin)	
118	DIF1	I	Digital Input Format 1 pin in Pin Control mode	Pull-down to DVSS (100 kΩ, typ)
	DZFR	O	Rch Zero Input Detect pin in Register Control mode (Internal pull-down pin)	
119	DIF2	I	Digital Input Format 2 pin in Pin Control mode	Hi-Z
	CAD0	I	Chip Address 0 pin in Register Control mode	
120	VTSEL	I	MCLK VIH/L Level Select pin. VTSEL = "L"; VIH = 1.36 V, VIL = 0.34 V VTSEL = "H"; VIH = 2.2 V, VIL = 0.8 V	Hi-Z
121-124	VREFHL1	I	L1ch High Level Reference Voltage Input pin.	Hi-Z
125-128	VREFLL1	I	L1ch Low Level Reference Voltage Input pin.	Hi-Z
-	TAB	-	The TAB on the bottom surface of the package should be connected to AVSS.	-

Note 2. All input pins except internal pull-up/down pins must not be left floating.
Note 3. The AK4499 must be powered down by the PDN pin when changing Pin Control/Register Control modes by the PSN pin.
Note 4. PCM mode, DSD mode, and EXDF mode are selectable in Register Control mode.

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