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National Semiconductor

February 2006

LM12454/LM12458/LM12H458
12-Bit + Sign Data Acquisition System with Self-Calibration

General Description

The LM12458, and LM12H458 are highly integrated Data Acquisition Systems. Operating on just 5V, they combine a fully-differential self-calibrating (correcting linearity and zero errors) 13-bit (12-bit + sign) analog-to-digital converter (ADC) and sample-and-hold (S/H) with extensive analog functions and digital functionality. Up to 32 consecutive conversions, using two's complement format, can be stored in an internal 32-word (16-bit wide) FIFO data buffer. An internal 8-word RAM can store the conversion sequence for up to eight acquisitions through the LM12(H)458's eight-input multiplexer. The obsolete LM12454 has a four-channel multiplexer, a differential multiplexer output, and a differential S/H input. The LM12(H)458 can also operate with 8-bit + sign resolution and in a supervisory "watchdog" mode that compares an input signal against two programmable limits.

Programmable acquisition times and conversion rates are possible through the use of internal clock-driven timers. The reference voltage input can be externally generated for absolute or ratiometric operation or can be derived using the internal 2.5V bandgap reference.

All registers, RAM, and FIFO are directly addressable through the high speed microprocessor interface to either an 8-bit or 16-bit data bus. The LM12(H)458 includes a direct memory access (DMA) interface for high-speed conversion data transfer.

Additional applications information can be found in applications notes AN-906, AN-947 and AN-949.

Key Specifications

(f_{CLK} = 5 MHz; 8 MHz, H)

■ Resolution	12-bit + sign or 8-bit + sign
■ 13-bit conversion time	8.8 µs, 5.5 µs (H) (max)
■ 9-bit conversion time	4.2 µs, 2.6 µs (H) (max)
■ 13-bit Through-put rate	88k samples/s (min), 140k samples/s (H) (min)
■ Comparison time ("watchdog" mode)	2.2 µs (max), 1.4 µs (H) (max)
■ ILE	±1 LSB (max)
■ V_{IN} range	GND to V_A^+
■ Power Consumption	30 mW, 34 mW (H) (max)
■ Stand-by mode	50 µW (typ)
■ Single supply	3V to 5.5V

Features

- Three operating modes: 12-bit + sign, 8-bit + sign, and "watchdog"
- Single-ended or differential inputs
- Built-in Sample-and-Hold and 2.5V bandgap reference
- Instruction RAM and event sequencer
- 8-channel multiplexer
- 32-word conversion FIFO
- Programmable acquisition times and conversion rates
- Self-calibration and diagnostic mode
- 8- or 16-bit wide data bus microprocessor or DSP interface

Applications

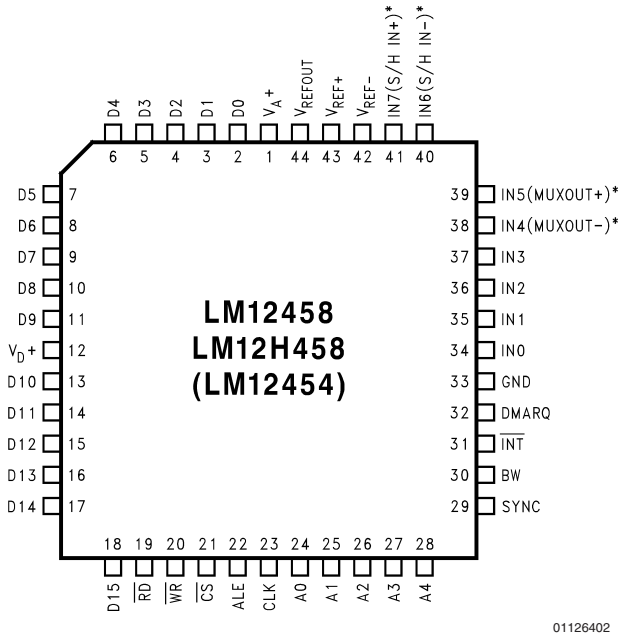
- Data Logging
- Instrumentation
- Process Control
- Energy Management
- Inertial Guidance

Ordering Information

Guaranteed Clock Freq (min)	Order Part Number	NS Package
8 MHz	LM12H458CIV LM12H458CIVX LM12H458CIVF	V44A (PLCC) V44A (PLCC) (Tape and Reel) VGZ44A (PQFP)
5 MHz	LM12454CIV * LM12458CIV LM12458CIVX LM12458CIVF *	V44A (PLCC) V44A (PLCC) V44A (PLCC) (Tape and Reel) VGZ44A (PQFP)

* These products are obsolete and shown for reference only.

Connection Diagrams



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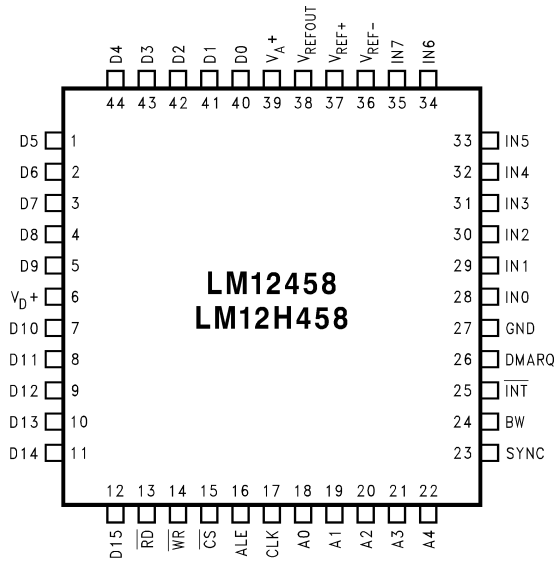
* Pin names in ( ) apply to the obsolete LM12454 and LM12H454.

Order Number LM12454CIV,
LM12458CIV or LM12H458CIV
See NS Package Number V44A



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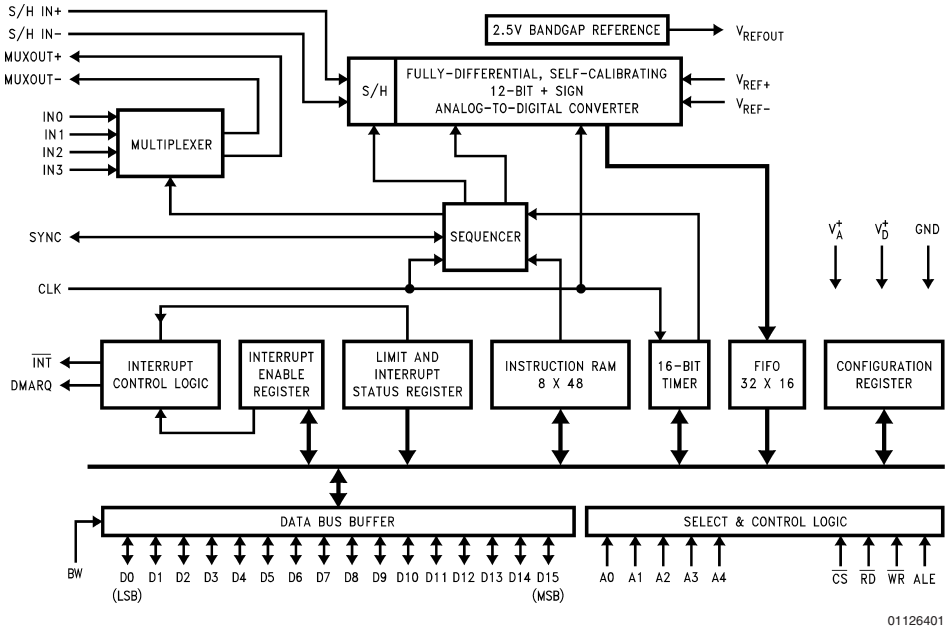
Order Number LM12458CIVF or LM12H458CIVF
NS Package Number VGZ44A

Functional Diagrams

LM12454



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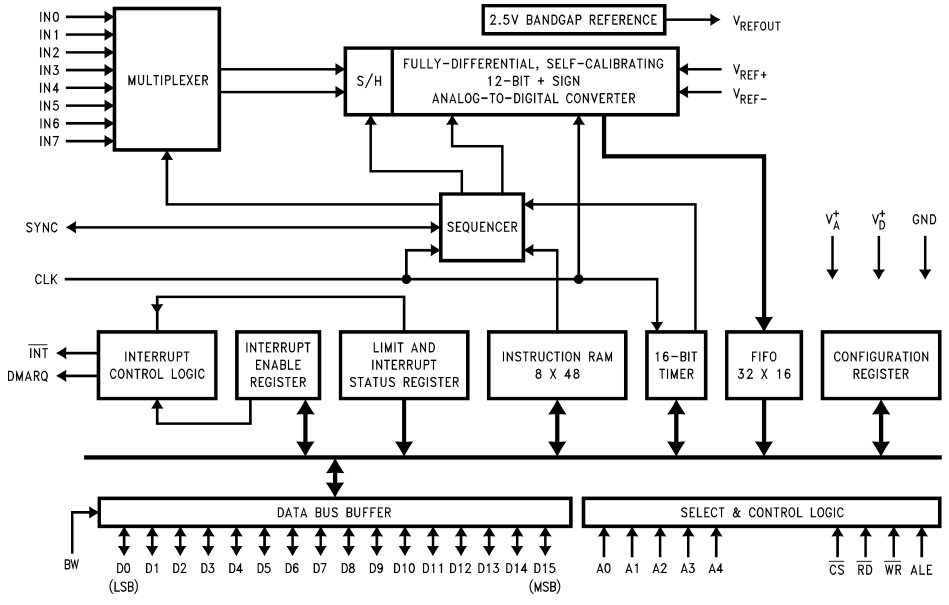
The LM12(H)454 is obsolete

LM12(H)458



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Absolute Maximum Ratings

(Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_A+ and V_D+)	6.0V
Voltage at Input and Output Pins, except analog inputs	−0.3V to (V^+ + 0.3V)
Voltage at Analog Inputs	− 5V to (V^+ + 5V)
$\lvert V_A+ - V_D+\rvert$	300 mV
Input Current at Any Pin (Note 3)	±5 mA
Package Input Current (Note 3)	±20 mA
Power Dissipation, PQFP (T_A = 25˚C) (Note 4)	875 mW
Storage Temperature	−65˚C to +150˚C
Lead Temperature	
PQFP, Infrared, 15 sec.	+300˚C
PLCC, Solder, 10 sec.	+250˚C
ESD Susceptibility (Note 5)	1.5 kV

See AN-450 “Surface Mounting Methods and Their Effect on Product Reliability” for other methods of soldering surface mount devices.

Operating Ratings (Notes 1, 2)

Temperature Range ($T_{min} \le T_A \le T_{max}$)	$-40˚C \le T_A \le 85˚C$
Supply Voltage V_A+, V_D+	3.0V to 5.5V
$\lvert V_A+ - V_D+\rvert$	≤100 mV
V_{IN+} Input Range	$GND \le V_{IN+} \le V_A+$
V_{IN-} Input Range	$GND \le V_{IN-} \le V_A+$
V_{REF+} Input Voltage	$1V \le V_{REF+} \le V_A+$
V_{REF-} Input Voltage	$0V \le V_{REF-} \le V_{REF+} - 1V$
$V_{REF+} - V_{REF-}$	$1V \le V_{REF} \le V_A+$
V_{REF} Common Mode Range (Note 16)	$0.1\ V_A^+ \le V_{REFCM} \le 0.6\ V_A^+$
T_J(MAX)	150˚C

Reliability Information - Transistor Count

Device Type	Nmber
P-Chan MOS Transistor	12,232
N-Chan MOS Transistor	15,457
Parasitic Vertical Bipolar Junction Transistor	4
Parasitic Lateral Bipolar Junction Transistor	2
TOTAL Transistors	27,695

Package Thermal Resistances

Package	θ_{JA}
44-Lead PQFP	47˚C / W
44-Lead PLCC	50˚C / W

Converter Characteristics (Notes 6, 7, 8, 9)

The following specifications apply to the LM12454, LM12458, and LM12H458 for $V_A+ = V_D+ = 5V$, $V_{REF+} = 5V$, $V_{REF-} = 0V$, 12-bit + sign conversion mode, f_{CLK} = 8.0 MHz (LM12H458) or f_{CLK} = 5.0 MHz (LM12454/8), $R_S = 25\Omega$, source impedance for V_{REF+} and $V_{REF-} \le 25\Omega$, fully-differential input with fixed 2.5V common-mode voltage, and minimum acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25˚C$.

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units
ILE	Integral Linearity Error (Notes 12, 17)	After Auto-Cal	±1/2	**±1**	LSB (max)
TUE	Total Unadjusted Error(Note 12)	After Auto-Cal	±1		LSB
	Resolution with No Missing Codes (Note 12)	After Auto-Cal		**13**	Bits (max)
DNL	Differential Non-Linearity	After Auto-Cal		**±¾**	LSB (max)
	Zero Error (Notes 13, 17)	After Auto-Cal LM12H458	 ±1/2	**±1** **±1.5**	 LSB (max)
	Positive Full-Scale Error (Notes 12, 17)	After Auto-Cal	±1/2	**±2**	LSB (max)
	Negative Full-Scale Error (Notes 12, 17)	After Auto-Cal	±1/2	**±2**	LSB (max)
	DC Common Mode Error (Note 14)		±2	**±3.5**	LSB (max)
ILE	8-Bit + Sign and “Watchdog” Mode Integral Linearity Error (Note 12)			**±1/2**	LSB (max)
TUE	8-Bit + Sign and “Watchdog” Mode Total Unadjusted Error	After Auto-Zero	±1/2	**±3/4**	LSB (max)
	8-Bit + Sign and “Watchdog” Mode Resolution with No Missing Codes			**9**	Bits (max)

Converter Characteristics (Notes 6, 7, 8, 9) (Continued)

The following specifications apply to the LM12454, LM12458, and LM12H458 for $V_A+ = V_D+ = 5V$, $V_{REF+} = 5V$, $V_{REF-} = 0V$, 12-bit + sign conversion mode, $f_{CLK} = 8.0$ MHz (LM12H458) or $f_{CLK} = 5.0$ MHz (LM12454/8), $R_S = 25\Omega$, source impedance for V_{REF+} and $V_{REF-} \leq 25\Omega$, fully-differential input with fixed 2.5V common-mode voltage, and minimum acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25^\circ C$.

Symbol	Parameter		Conditions	Typical (Note 10)	Limits (Note 11)	Units
DNL	8-Bit + Sign and "Watchdog" Mode Differential Non-Linearity				**±3/4**	LSB (max)
	8-Bit + Sign and "Watchdog" Mode Zero Error		After Auto-Zero		**±1/2**	LSB (max)
	8-Bit + Sign and "Watchdog" Full-Scale Error				**±1/2**	LSB (max)
	8-Bit + Sign and "Watchdog" Mode DC Common Mode Error			±1/8		LSB
	Multiplexer Channel-to-Channel Matching			±0.05		LSB
V_{IN+}	Non-Inverting Input Range				**GND** **V_A+**	V (min) V (max)
V_{IN-}	Inverting Input Range				**GND** **V_A+**	V (min) V (max)
$V_{IN+} - V_{IN-}$	Differential Input Voltage Range				**$-V_A{}^+$** **V_A+**	V (min) V (max)
$\frac{V_{IN+} - V_{IN-}}{2}$	Common Mode Input Voltage Range				**GND** **V_A+**	V (min) V (max)
PSS	Power Supply Sensitivity (Note 15)	Zero Error	$V_A+ = V_D+ = 5V$ ±10%	±0.2	**±1.75**	LSB (max)
		Full-Scale Error	$V_{REF+} = 4.5V$, V_{REF-} = GND	±0.4	**±2**	LSB (max)
		Linearity Error		±0.2		LSB
C_{REF}	V_{REF+}/V_{REF-} Input Capacitance			85		pF
C_{IN}	Selected Multiplexer Channel Input Capacitance			75		pF

Converter AC Characteristics (Notes 6, 7, 8, 9)

The following specifications apply to the LM12454, LM12458, and LM12H458 for $V_A+ = V_D+ = 5V$, $V_{REF+} = 5V$, $V_{REF-} = 0V$, 12-bit + sign conversion mode, $f_{CLK} = 8.0$ MHz (LM12H458) or $f_{CLK} = 5.0$ MHz (LM12454/8), $R_S = 25\Omega$, source impedance for V_{REF+} and $V_{REF-} \leq 25\Omega$, fully-differential input with fixed 2.5V common-mode voltage, and minimum acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25^\circ C$.

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units
	Clock Duty Cycle		50	**40** **60**	% % (min) % (max)
t_C	Conversion Time	13-Bit Resolution, Sequencer State S5 (*Figure 15*)	44 (t_{CLK})	**44 (t_{CLK}) + 50 ns**	(max)
		9-Bit Resolution, Sequencer State S5 (*Figure 15*)	21 (t_{CLK})	**21 (t_{CLK}) + 50 ns**	(max)
t_A	Acquisition Time	Sequencer State S7 (*Figure 15*) Built-in minimum for 13-Bits	9 (t_{CLK})	**9 (t_{CLK}) + 50 ns**	(max)
		Built-in minimum for 9-Bits and "Watchdog" mode	2 (t_{CLK})	**2 (t_{CLK}) + 50 ns**	(max)
t_Z	Auto-Zero Time	Sequencer State S2 (*Figure 15*)	76 (t_{CLK})	**76 (t_{CLK}) + 50 ns**	(max)
t_{CAL}	Full Calibration Time	Sequencer State S2 (*Figure 15*)	4944 (t_{CLK})	**4944 (t_{CLK}) + 50 ns**	(max)
	Throughput Rate (Note 18)		89	**88**	kHz (min)
		LM12H458	142	**140**	kHz (min)

Converter AC Characteristics (Notes 6, 7, 8, 9) (Continued)

The following specifications apply to the LM12454, LM12458, and LM12H458 for $V_A+ = V_D+ = 5V$, $V_{REF+} = 5V$, $V_{REF-} = 0V$, 12-bit + sign conversion mode, $f_{CLK} = 8.0$ MHz (LM12H458) or $f_{CLK} = 5.0$ MHz (LM12454/8), $R_S = 25\Omega$, source impedance for V_{REF+} and $V_{REF-} \leq 25\Omega$, fully-differential input with fixed 2.5V common-mode voltage, and minimum acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25^\circ C$.

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units
t_{WD}	"Watchdog" Mode Comparison Time	Sequencer States S6, S4, and S5 (*Figure 15*)	11 (t_{CLK})	**11 (t_{CLK}) + 50 ns**	(max)
DSNR	Differential Signal-to-Noise Ratio	V_{IN} = ±5V			
		f_{IN} = 1 kHz	77.5		dB
		f_{IN} = 20 kHz	75.2		dB
		f_{IN} = 40 kHz	74.7		dB
SESNR	Single-Ended Signal-to-Noise Ratio	V_{IN} = 5 V_{p-p}			
		f_{IN} = 1 kHz	69.8		dB
		f_{IN} = 20 kHz	69.2		dB
		f_{IN} = 40 kHz	66.6		dB
DSINAD	Differential Signal-to-Noise + Distortion Ratio	V_{IN} = ±5V			
		f_{IN} = 1 kHz	76.9		dB
		f_{IN} = 20 kHz	73.9		dB
		f_{IN} = 40 kHz	70.7		dB
SESINAD	Single-Ended Signal-to-Noise + Distortion Ratio	V_{IN} = 5 V_{p-p}			
		f_{IN} = 1 kHz	69.4		dB
		f_{IN} = 20 kHz	68.3		dB
		f_{IN} = 40 kHz	65.7		dB
DTHD	Differential Total Harmonic Distortion	V_{IN} = ±5V			
		f_{IN} = 1 kHz	–85.8		dB
		f_{IN} = 20 kHz	–79.9		dB
		f_{IN} = 40 kHz	–72.9		dB
SETHD	Single-Ended Total Harmonic Distortion	V_{IN} = 5 V_{p-p}			
		f_{IN} = 1 kHz	–80.3		dB
		f_{IN} = 20 kHz	–75.6		dB
		f_{IN} = 40 kHz	–72.8		dB
DENOB	Differential Effective Number of Bits	V_{IN} = ±5V			
		f_{IN} = 1 kHz	12.6		Bits
		f_{IN} = 20 kHz	12.2		Bits
		f_{IN} = 40 kHz	12.1		Bits
SEENOB	Single-Ended Effective Number of Bits	V_{IN} = 5 V_{p-p}			
		f_{IN} = 1 kHz	11.3		Bits
		f_{IN} = 20 kHz	11.2		Bits
		f_{IN} = 40 kHz	10.8		Bits
DSFDR	Differential Spurious Free Dynamic Range	V_{IN} = ±5V			
		f_{IN} = 1 kHz	87.2		dB
		f_{IN} = 20 kHz	78.9		dB
		f_{IN} = 40 kHz	72.8		dB
	Multiplexer Channel-to-Channel Crosstalk	V_{IN} = 5 V_{P-P}, f_{IN} = 40 kHz, LM12454 MUXOUT Only	–76		dB
		V_{IN} = 5 V_{P-P}, f_{IN} = 40 kHz, LM12(H)458 MUX plus Converter	–78		dB
t_{PU}	Power-Up Time		10		ms
t_{WU}	Wake-Up Time		10		ms

DC Characteristics (Notes 6, 7, 8)

The following specifications apply to the LM12454, LM12458, and LM12H458 for $V_A+ = V_D+ = 5V$, $V_{REF+} = 5V$, $V_{REF-} = 0V$, $f_{CLK} = 8.0$ MHz (LM12H454/8) or $f_{CLK} = 5.0$ MHz (LM12458), and minimum acquisition time unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25^\circ C$.

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units
I_D+	V_D+ Supply Current	$\overline{CS}$ = "1"			
		LM12454/8	0.55	**1.0**	mA (max)
		LM12H458	0.55	**1.2**	mA (max)
I_A+	V_A+ Supply Current	$\overline{CS}$ = "1"			
		LM12454/8	3.1	**5.0**	mA (max)
		LM12H458	3.1	**5.5**	mA (max)
I_{ST}	Stand-By Supply Current (I_D+) + (I_A+) [Power-Down Mode Selected]	Clock Stopped	10		µA (max)
		8 MHz Clock	40		µA (max)
	Multiplexer ON-Channel Leakage Current	$V_A+ = 5.5V$, ON-Channel = 5.5V, OFF-Channel = 0V	0.1	**0.3**	µA (max)
		ON-Channel = 0V, OFF-Channel = 5.5V	0.1	**0.3**	µA (max)
	Multiplexer OFF-Channel Leakage Current	$V_A+ = 5.5V$, ON-Channel = 5.5V, OFF-Channel = 0V	0.1	**0.3**	µA (max)
		ON-Channel = 0V, OFF-Channel = 5.5V	0.1	**0.3**	µA (max)
R_{ON}	Multiplexer ON-Resistance	LM12454			
		$V_{IN} = 5V$	800	**1500**	Ω(max)
		$V_{IN} = 2.5V$	850	**1500**	Ω(max)
		$V_{IN} = 0V$	760	**1500**	Ω(max)
	Multiplexer Channel-to-Channel R_{ON} matching	LM12454			
		$V_{IN} = 5V$	±1.0%	**±3.0%**	(max)
		$V_{IN} = 2.5V$	±1.0%	**±3.0%**	(max)
		$V_{IN} = 0V$	±1.0%	**±3.0%**	(max)

Internal Reference Characteristics (Notes 6, 7)

The following specifications apply to the LM12454, LM12458, and LM12H458 for $V_A+ = V_D+ = 5V$ unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25^\circ C$.

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units
V_{REFOUT}	Internal Reference Output Voltage		2.5	**2.5 ±4%**	V (max)
$\Delta V_{REF}/\Delta T$	Internal Reference Temperature Coefficient		40		ppm/°C
$\Delta_{REF}/\Delta I_L$	Internal Reference Load Regulation	Sourcing ($0 < I_L \leq +4$ mA)		**0.2**	%/mA (max)
		Sinking ($-1 \leq I_{IL} < 0$ mA)		**1.2**	%/mA (max)
ΔV_{REF}	Line Regulation	$4.5V \leq V_A+ \leq 5.5V$	3	**20**	mV (max)
I_{SC}	Internal Reference Short Circuit Current	$V_{REFOUT} = 0V$	13	**25**	mA (max)
$\Delta V_{REF}/\Delta t$	Long Term Stability		200		ppm/kHr
t_{SU}	Internal Reference Start-Up Time	$V_A+ = V_D+ = 0V \rightarrow 5V$, $C_L = 100$ µF	10		ms

Digital Characteristics (Notes 6, 7)

The following specifications apply to the LM12454, LM12458, and LM12H458 for $V_A+ = V_D+ = 5V$, unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25^\circ C$.

Symbol	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units
$V_{IN(1)}$	Logical "1" Input Voltage	$V_A+ = V_D+ = 5.5V$		**2.0**	V (min)
$V_{IN(0)}$	Logical "0" Input Voltage	$V_A+ = V_D+ = 4.5V$		**0.8**	V (max)
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN} = 5V$	0.005	**1.0**	µA (max)
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN} = 0V$	−0.005	**−1.0**	µA (max)
C_{IN}	D0–D15 Input Capacitance		6		pF
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_A+ = V_D+ = 4.5V$ $I_{OUT} = -360$ µA $I_{OUT} = -10$ µA		 **2.4** **4.25**	 V (min) V (min)
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_A+ = V_D+ = 4.5V$ $I_{OUT} = 1.6$ mA		**0.4**	V (max)
I_{OUT}	TRI-STATE® Output Leakage Current	$V_{OUT} = 0V$ $V_{OUT} = 5V$	−0.01 0.01	**−3.0** **3.0**	µA (max) µA (max)

Digital Timing Characteristics (Notes 6, 7, 8)

The following specifications apply to the LM12454, LM12458, and LM12H458 for $V_A+ = V_D+ = 5V$, $t_r = t_f = 3$ ns, and $C_L = 100$ pF on data I/O, $\overline{INT}$ and DMARQ lines unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}**; all other limits $T_A = T_J = 25^\circ C$.

Symbol (See *Figures 8, 9, 10*)	Parameter	Conditions	Typical (Note 10)	Limits (Note 11)	Units
1, 3	$\overline{CS}$ or Address Valid to ALE Low Set-Up Time			**40**	ns (min)
2, 4	$\overline{CS}$ or Address Valid to ALE Low Hold Time			**20**	ns (min)
5	ALE Pulse Width			**45**	ns (min)
6	$\overline{RD}$ High to Next ALE High			**35**	ns (min)
7	ALE Low to $\overline{RD}$ Low			**20**	ns (min)
8	$\overline{RD}$ Pulse Width			**100**	ns (min)
9	$\overline{RD}$ High to Next $\overline{RD}$ or $\overline{WR}$ Low			**100**	ns (min)
10	ALE Low to $\overline{WR}$ Low			**20**	ns (min)
11	$\overline{WR}$ Pulse Width			**60**	ns (min)
12	$\overline{WR}$ High to Next ALE High			**75**	ns (min)
13	$\overline{WR}$ High to Next $\overline{RD}$ or $\overline{WR}$ Low			**140**	ns (min)
14	Data Valid to $\overline{WR}$ High Set-Up Time			**40**	ns (min)
15	Data Valid to $\overline{WR}$ High Hold Time			**30**	ns (min)
16	$\overline{RD}$ Low to Data Bus Out of TRI-STATE		40	**10** **70**	ns (min) ns (max)
17	$\overline{RD}$ High to TRI-STATE	$R_L = 1$ kΩ	30	**10** **110**	ns (min) ns (max)
18	$\overline{RD}$ Low to Data Valid (Access Time)		30	**10** **80**	ns (min) ns (max)
20	Address Valid or $\overline{CS}$ Low to $\overline{RD}$ Low			**20**	ns (min)
21	Address Valid or $\overline{CS}$ Low to $\overline{WR}$ Low			**20**	ns (min)
19	Address Invalid from $\overline{RD}$ or $\overline{WR}$ High			**10**	ns (min)
22	$\overline{INT}$ High from $\overline{RD}$ Low		30	**10** **60**	ns (min) ns (max)
23	DMARQ Low from $\overline{RD}$ Low		30	**10** **60**	ns (min) ns (max)

Digital Timing Characteristics (Notes 6, 7, 8) (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

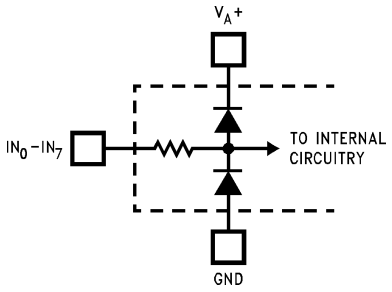
Note 2: All voltages are measured with respect to GND, unless otherwise specified.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply rails (V_{IN} < GND or V_{IN} > (V_A+ or V_D+)), the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating allows the voltage at any four pins, with an input current of 5 mA, to simultaneously exceed the power supply voltages.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature).

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 6: Two on-chip diodes are tied to each analog input through a series resistor, as shown below. Input voltage magnitude up to 5V above V_A+ or 5V below GND will not damage the LM12454 or the LM12(H)458. However, errors in the A/D conversion can occur if these diodes are forward biased by more than 100 mV. As an example, if V_A+ is 4.5 V_{DC}, full-scale input voltage must be ≤4.6 V_{DC} to ensure accurate conversions.



01126403

Note 7: V_A+ and V_D+ must be connected together to the same power supply voltage and bypassed with separate capacitors at each V^+ pin to assure conversion/comparison accuracy.

Note 8: Accuracy is guaranteed when operating at f_{CLK} = 5 MHz for the LM12454/8 and f_{CLK} = 8 MHz for the LM12H458.

Note 9: With the test condition for V_{REF} (V_{REF+} – V_{REF-}) given as +5V, the 12-bit LSB is 1.22 mV and the 8-bit/"Watchdog" LSB is 19.53 mV.

Note 10: Typical figures are at T_A = 25˚C and represent most likely parametric norm.

Note 11: Limits are guaranteed to National's AOQL (Average Output Quality Level).

Note 12: Positive integral linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive full-scale and zero. For negative integral linearity error the straight line passes through negative full-scale and zero. (See *Figure 6 Figure 7*).

Note 13: Zero error is a measure of the deviation from the mid-scale voltage (a code of zero), expressed in LSB. It is the worst-case value of the code transitions between –1 to 0 and 0 to +1 (see *Figure 8*).

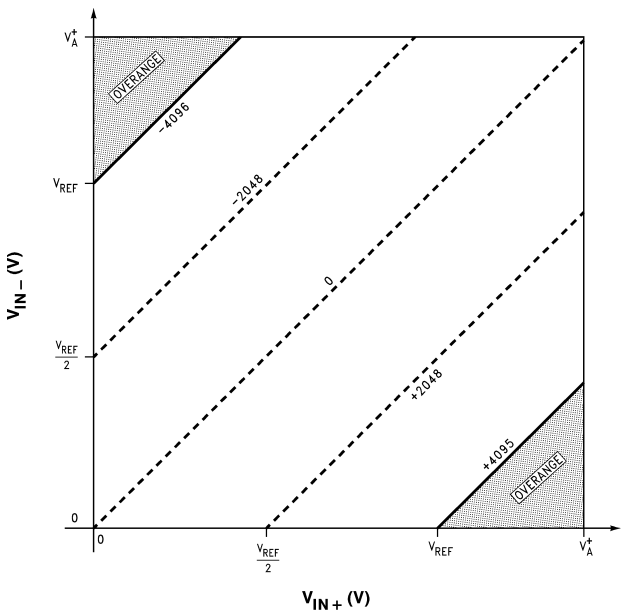
Note 14: The DC common-mode error is measured with both inputs shorted together and driven from 0V to 5V. The measured value is referred to the resulting output value when the inputs are driven with a 2.5V signal.

Note 15: Power Supply Sensitivity is measured after Auto-Zero and/or Auto-Calibration cycle has been completed with V_A+ and V_D+ at the specified extremes.

Note 16: V_{REFCM} (Reference Voltage Common Mode Range) is defined as (V_{REF+} + V_{REF-})/2.

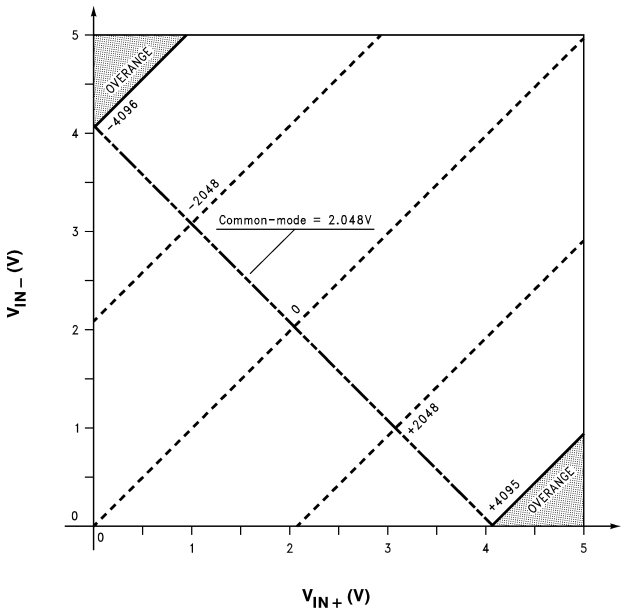
Note 17: The LM12(H)454/8's self-calibration technique ensures linearity and offset errors as specified, but noise inherent in the self-calibration process will result in a repeatability uncertainty of ±0.10 LSB.

Note 18: The Throughput Rate is for a single instruction repeated continuously. Sequencer states 0 (1 clock cycle), 1 (1 clock cycle), 7 (9 clock cycles) and 5 (44 clock cycles) are used (see *Figure 15*). One additional clock cycle is used to read the conversion result stored in the FIFO, for a total of 56 clock cycles per conversion. The Throughput Rate is f_{CLK} (MHz)/N, where N is the number of clock cycles/conversion.



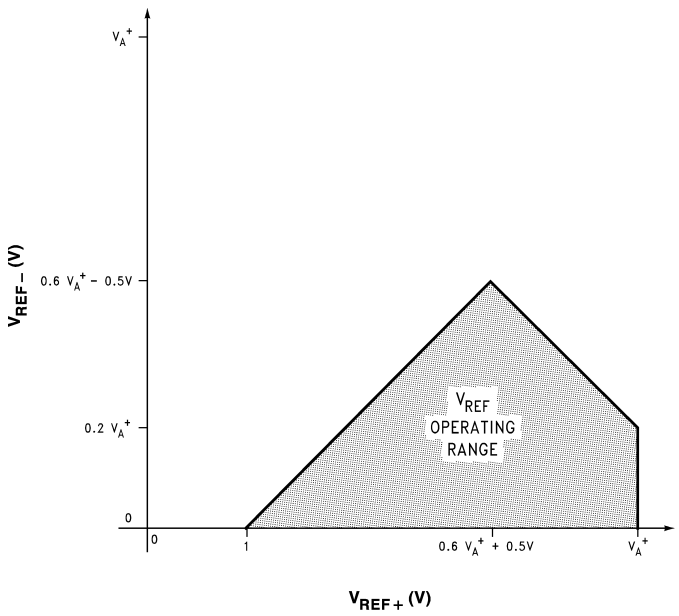
$V_{REF} = V_{REF+} - V_{REF-}$
$V_{IN} = V_{IN+} - V_{IN-}$
$GND \leq V_{IN+} \leq V_A+$
$GND \leq V_{IN-} \leq V_A+$

FIGURE 1. The General Case of Output Digital Code vs. the Operating Input Voltage Range



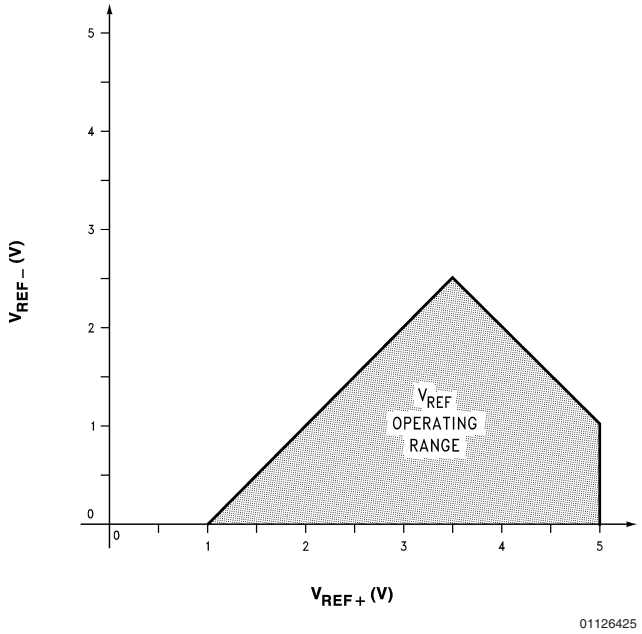
$V_{REF+} - V_{REF-} = 4.096V$
$V_{IN} = V_{IN+} - V_{IN-}$
$GND \leq V_{IN+} \leq V_A+$
$GND \leq V_{IN-} \leq V_A+$

FIGURE 2. Specific Case of Output Digital Code vs. the Operating Input Voltage Range for V_{REF} = 4.096V



$V_{REF} = V_{REF+} - V_{REF-}$

FIGURE 3. The General Case of the V_{REF} Operating Range



$V_{REF} = V_{REF+} - V_{REF-}$
$V_A+ = 5V$

FIGURE 4. The Specific Case of the V_{REF} Operating Range for $V_A+ = 5V$

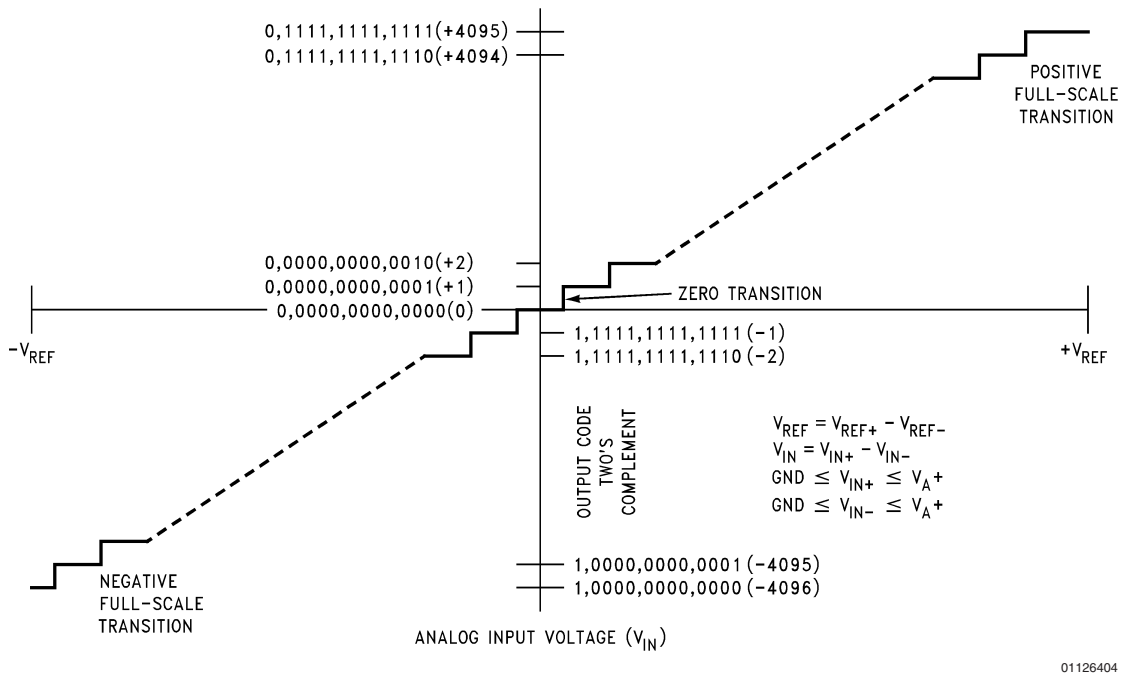


FIGURE 5. Transfer Characteristic

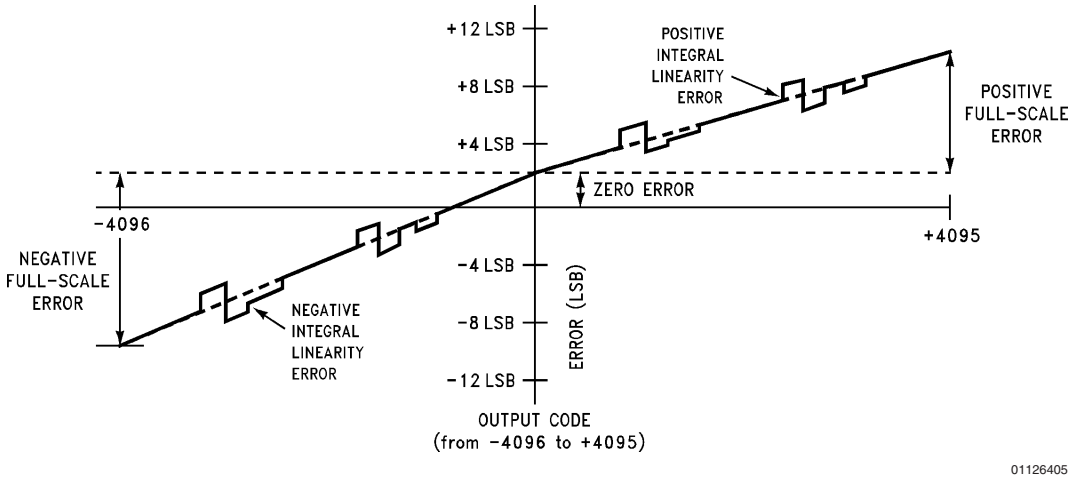


FIGURE 6. Simplified Error Curve vs. Output Code without Auto-Calibration or Auto-Zero Cycles

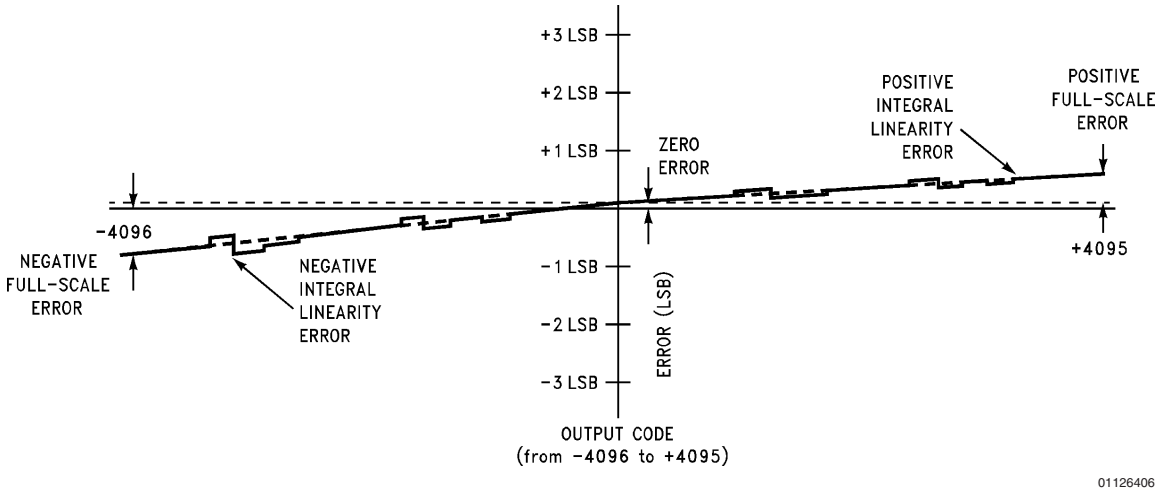


FIGURE 7. Simplified Error Curve vs. Output Code after Auto-Calibration Cycle

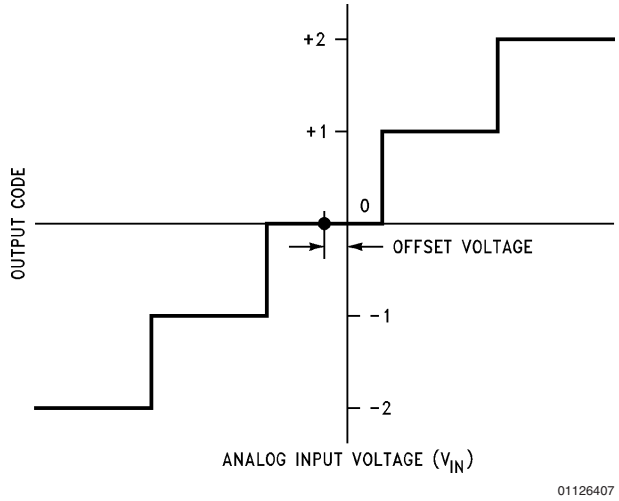
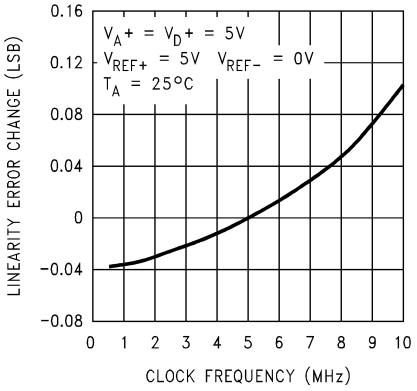


FIGURE 8. Offset or Zero Error Voltage

Typical Performance Characteristics

(Note 9) The following curves apply for 12-bit + sign mode after auto-calibration unless otherwise specified. The performance for 8-bit + sign and "watchdog" modes is equal to or better than shown.

Linearity Error Change vs. Clock Frequency



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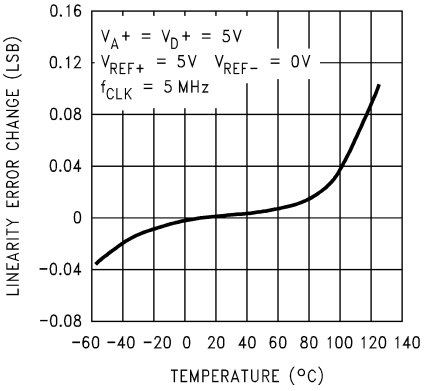
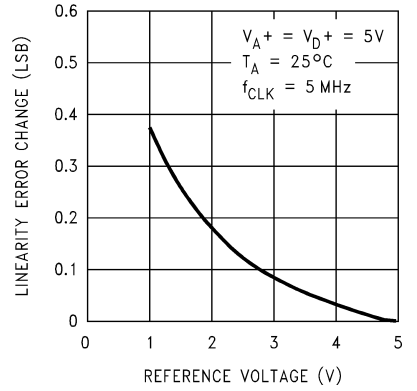
Linearity Error Change vs. Temperature



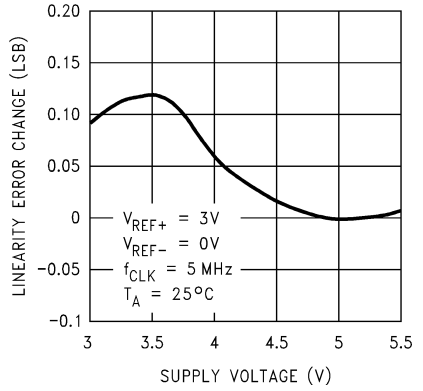
01126438

Linearity Error Change vs. Reference Voltage



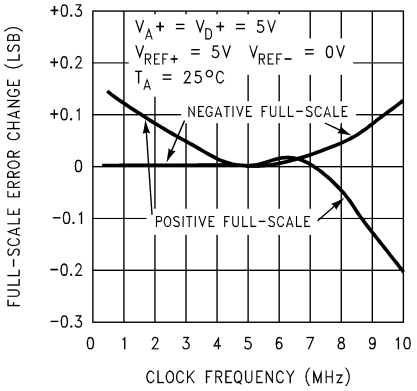
01126439

Linearity Error Change vs. Supply Voltage



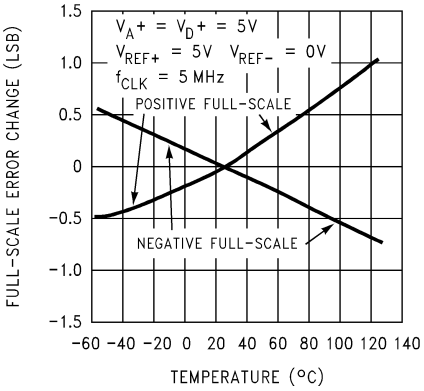
01126440

Full-Scale Error Change vs. Clock Frequency



01126441

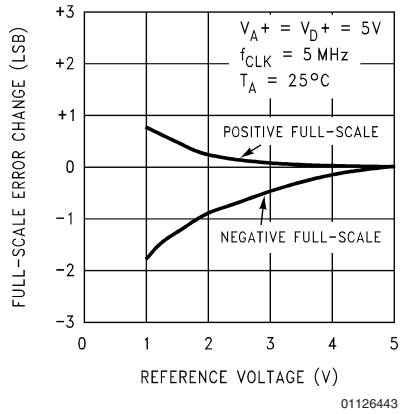
Full-Scale Error Change vs. Temperature



01126442

Typical Performance Characteristics (Note 9) The following curves apply for 12-bit + sign mode after auto-calibration unless otherwise specified. The performance for 8-bit + sign and "watchdog" modes is equal to or better than shown. (Continued)

Full-Scale Error Change vs. Reference Voltage



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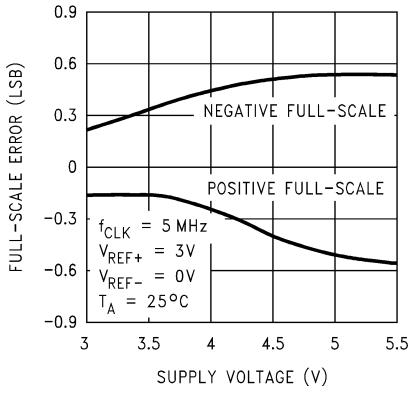
Full-Scale Error vs. Supply Voltage



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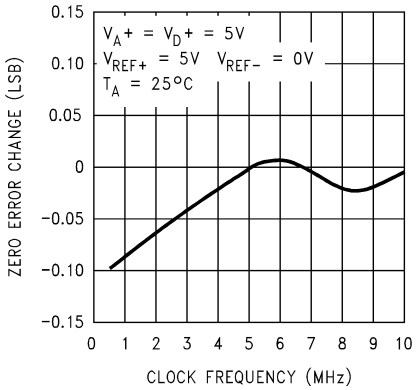
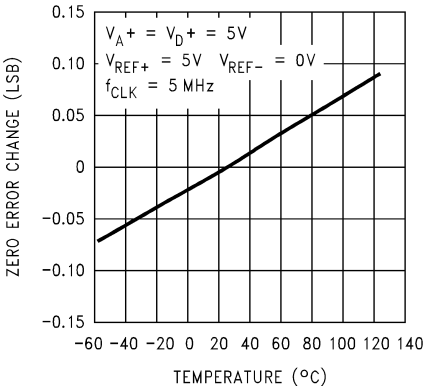
Zero Error Change vs. Clock Frequency



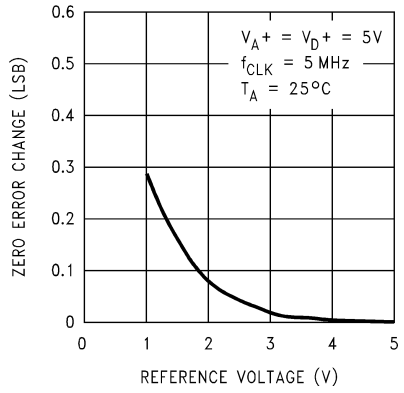
01126445

Zero Error Change vs. Temperature



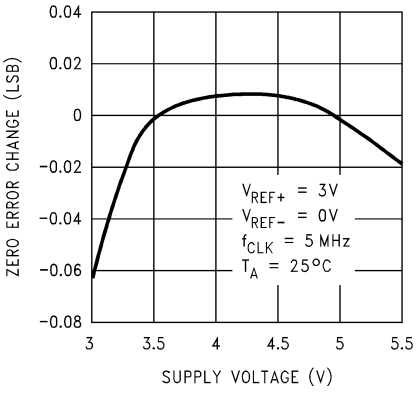
01126446

Zero Error Change vs. Reference Voltage



01126447

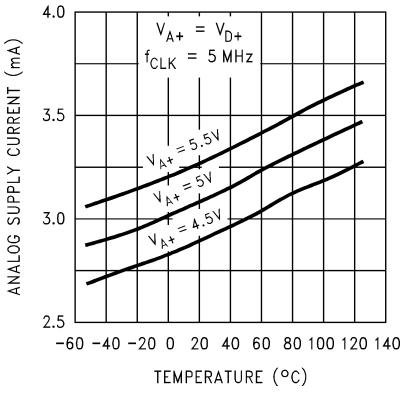
Zero Error Change vs. Supply Voltage



01126448

Typical Performance Characteristics (Note 9) The following curves apply for 12-bit + sign mode after auto-calibration unless otherwise specified. The performance for 8-bit + sign and "watchdog" modes is equal to or better than shown. (Continued)

Analog Supply Current vs. Temperature



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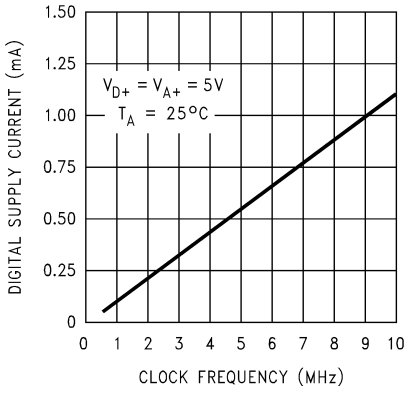
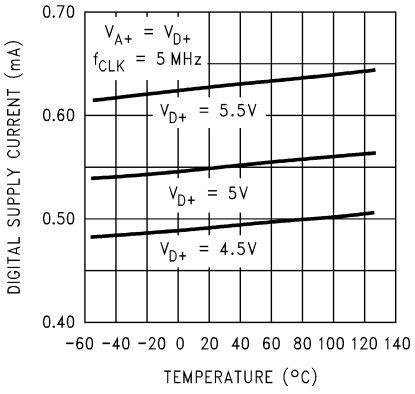
Digital Supply Current vs. Clock Frequency



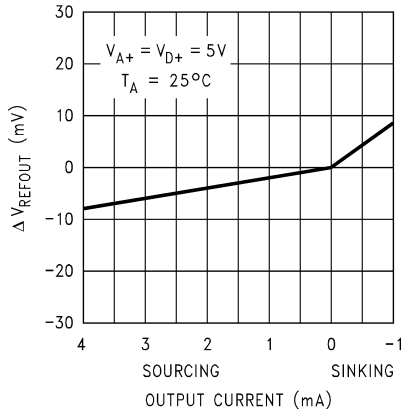
01126450

Digital Supply Current vs. Temperature



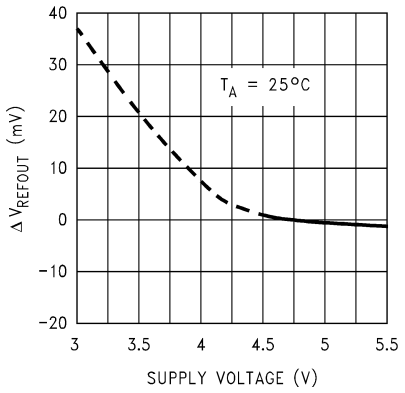
01126451

V_{REFOUT} Load Regulation



01126452

V_{REFOUT} Line Regulation

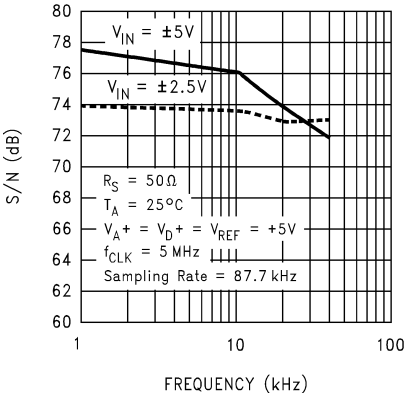


01126453

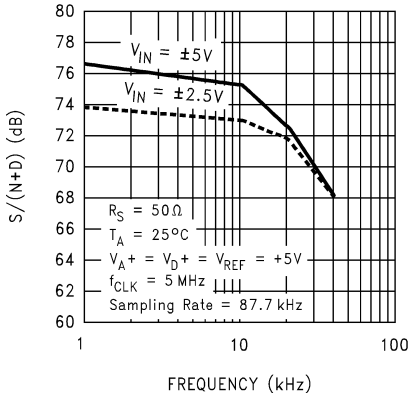
Typical Dynamic Performance Characteristics

The following curves apply for 12-bit + sign mode after auto-calibration unless otherwise specified.

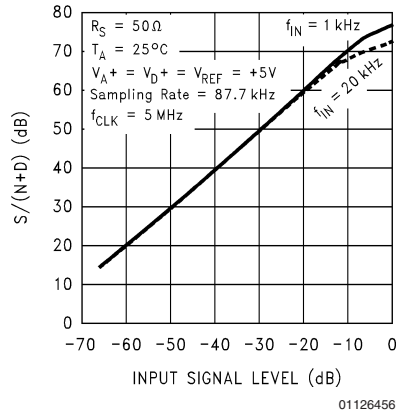
Bipolar Signal-to-Noise Ratio vs. Input Frequency



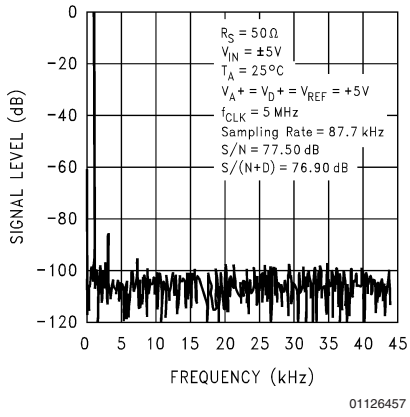
Bipolar Signal-to-Noise + Distortion Ratio vs. Input Frequency



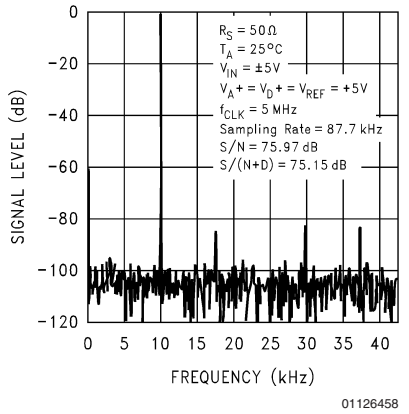
Bipolar Signal-to-Noise + Distortion Ratio vs. Input Signal Level



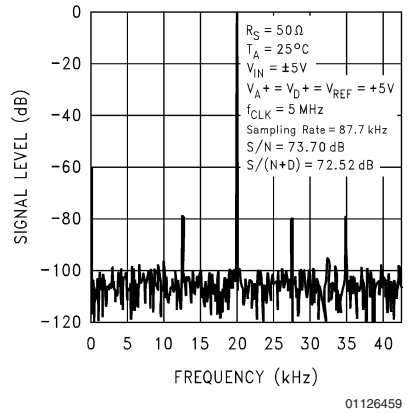
Bipolar Spectral Response with 1.028 kHz Sine Wave Input



Bipolar Spectral Response with 10 kHz Sine Wave Input



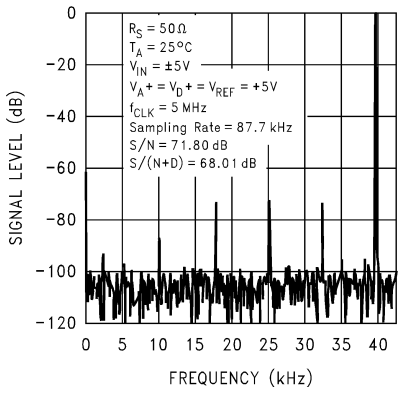
Bipolar Spectral Response with 20 kHz Sine Wave Input



Typical Dynamic Performance Characteristics

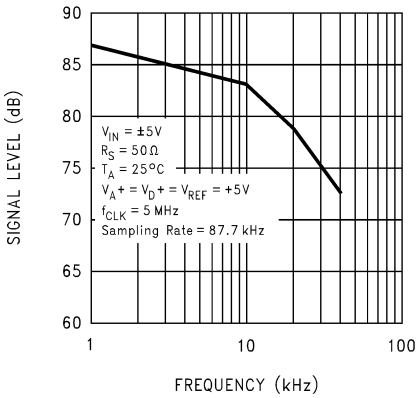
The following curves apply for 12-bit + sign mode after auto-calibration unless otherwise specified. (Continued)

Bipolar Spectral Response with 40 kHz Sine Wave Input



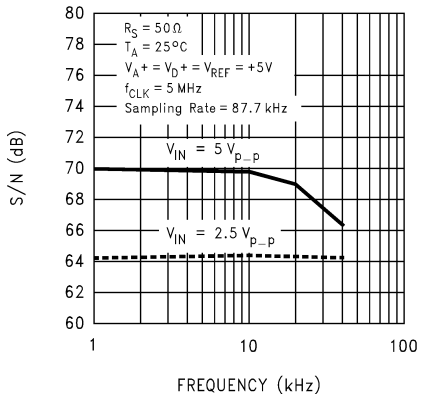
01126460

Bipolar Spurious Free Dynamic Range



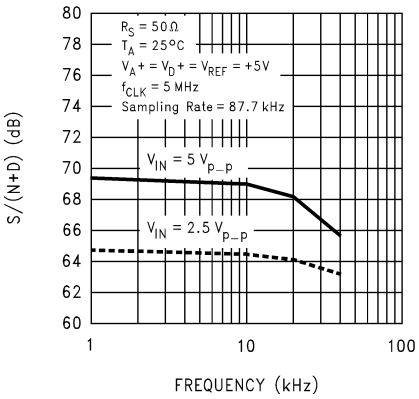
01126461

Unipolar Signal-to-Noise Ratio vs. Input Frequency



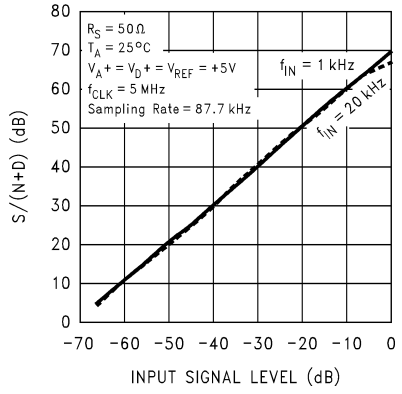
01126462

Unipolar Signal-to-Noise + Distortion Ratio vs. Input Frequency



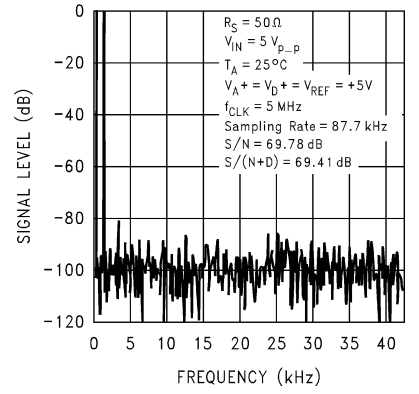
01126463

Unipolar Signal-to-Noise + Distortion Ratio vs. Input Signal Level



01126464

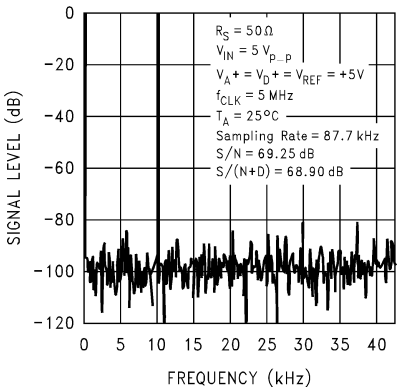
Unipolar Spectral Response with 1.028 kHz Sine Wave Input



01126465

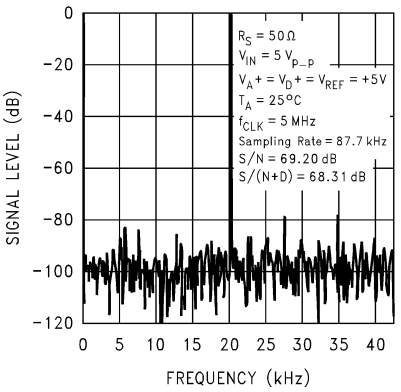
Typical Dynamic Performance Characteristics The following curves apply for 12-bit + sign mode after auto-calibration unless otherwise specified. (Continued)

Unipolar Spectral Response with 10 kHz Sine Wave Input



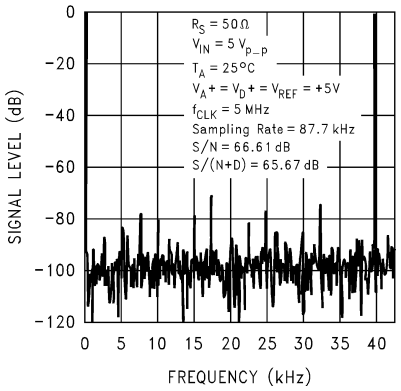
01126466

Unipolar Spectral Response with 20 kHz Sine Wave Input



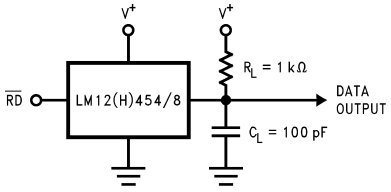
01126467

Unipolar Spectral Response with 40 kHz Sine Wave Input

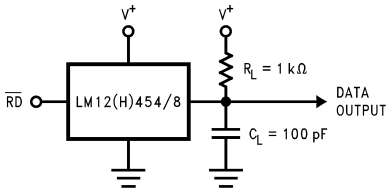


01126468

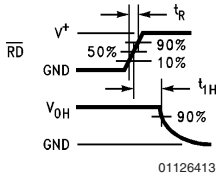
Test Circuits and Waveforms



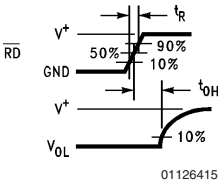
01126412



01126414



01126413



01126415

FIGURE 9. TRI-STATE Test Circuits and Waveforms

Timing Diagrams

$V_A+ = V_D+ = +5V$, $t_R = t_F = 3$ ns, $C_L = 100$ pF for the $\overline{INT}$, DMARQ, D0–D15 outputs.

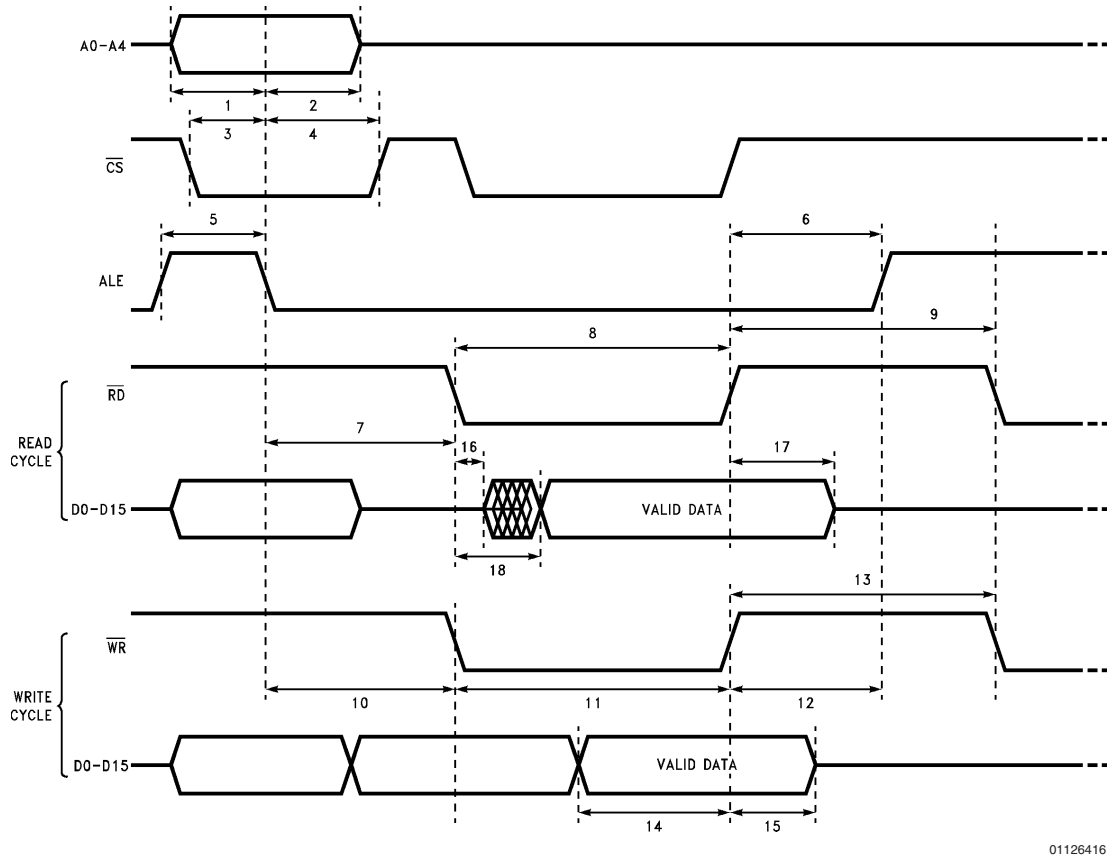


FIGURE 10. Multiplexed Data Bus

1, 3: $\overline{CS}$ or Address valid to ALE low set-up time.
2, 4: $\overline{CS}$ or Address valid to ALE low hold time.
5: ALE pulse width
6: $\overline{RD}$ high to next ALE high
7: ALE low to $\overline{RD}$ low
8: $\overline{RD}$ pulse width
9: $\overline{RD}$ high to next $\overline{RD}$ or $\overline{WR}$ low
10: ALE low to $\overline{WR}$ low
11: $\overline{WR}$ pulse width
12: $\overline{WR}$ high to next ALE high
13: $\overline{WR}$ high to next $\overline{WR}$ or $\overline{RD}$ low
14: Data valid to $\overline{WR}$ high set-up time
15: Data valid to $\overline{WR}$ high hold time
16: $\overline{RD}$ low to data bus out of TRI-STATE
17: $\overline{RD}$ high to TRI-STATE
18: $\overline{RD}$ low to data valid (access time)

Timing Diagrams $V_A+ = V_D+ = +5V$, $t_R = t_F = 3$ ns, $C_L = 100$ pF for the $\overline{INT}$, DMARQ, D0–D15 outputs. (Continued)

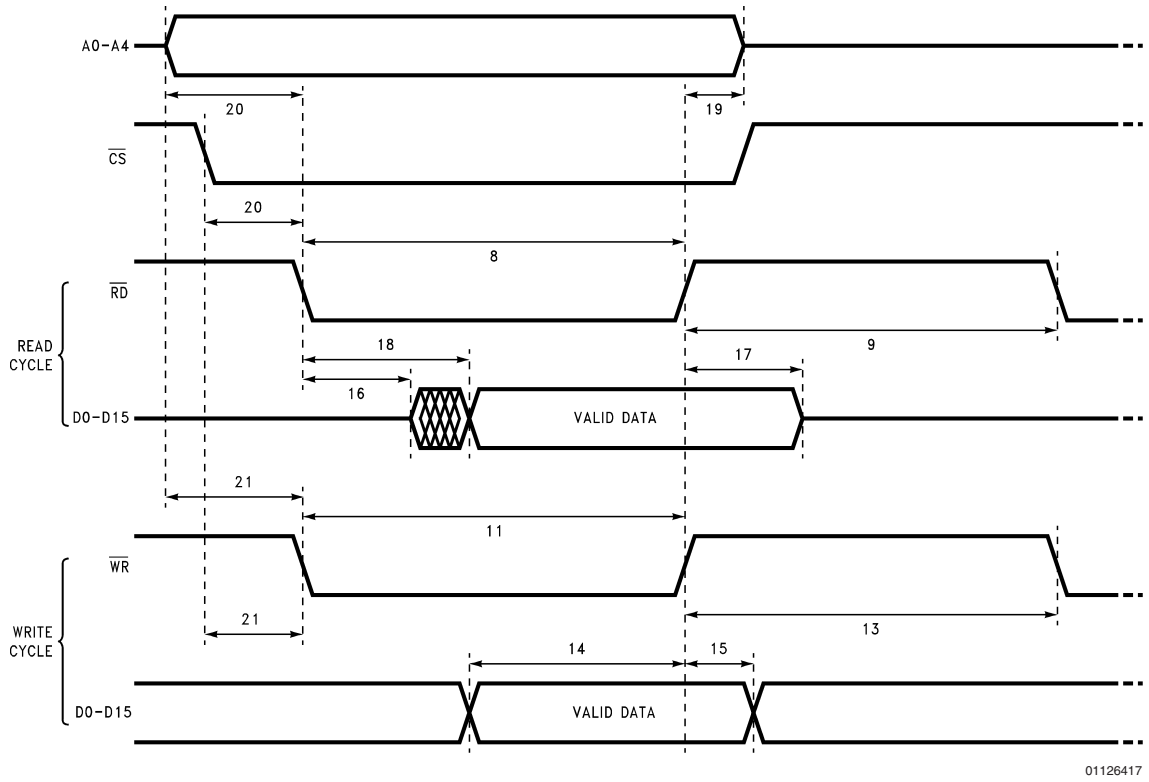


FIGURE 11. Non-Multiplexed Data Bus (ALE = 1)

8: $\overline{RD}$ pulse width
9: $\overline{RD}$ high to next $\overline{RD}$ or $\overline{WR}$ low
11: $\overline{WR}$ pulse width
13: $\overline{WR}$ high to next $\overline{WR}$ or $\overline{RD}$ low
14: Data valid to $\overline{WR}$ high set-up time
15: Data valid to $\overline{WR}$ high hold time
16: $\overline{RD}$ low to data bus out of TRI-STATE
17: $\overline{RD}$ high to TRI-STATE
18: $\overline{RD}$ low to data valid (access time)
19: Address invalid from $\overline{RD}$ or $\overline{WR}$ high (hold time)
20: $\overline{CS}$ low or address valid to $\overline{RD}$ low
21: $\overline{CS}$ low or address valid to $\overline{WR}$ low
$V_A+ = V_D+ = +5V$, $t_R = t_F = 3$ ns, $C_L = 100$ pF for the $\overline{INT}$, DMARQ, D0–D15 outputs.

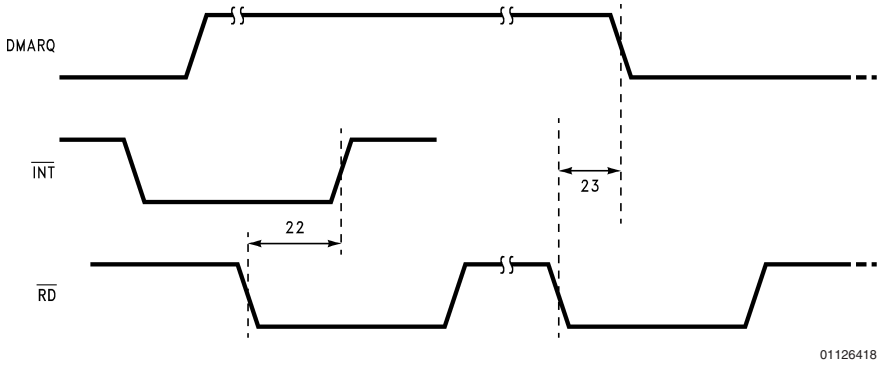


FIGURE 12. Interrupt and DMARQ

22: $\overline{INT}$ high from $\overline{RD}$ low
23: DMARQ low from $\overline{RD}$ low

Pin Descriptions

V_A+ V_D+ Analog and digital supply voltage pins. The LM12(H)454/8's supply voltage operating range is +3.0V to +5.5V. Accuracy is guaranteed only if V_A+ and V_D+ are connected to the same power supply. Each pin should have a parallel combination of 10 µF (electrolytic or tantalum) and 0.1 µF (ceramic) bypass capacitors connected between it and ground.

D0–D15 The internal data input/output TRI-STATE buffers are connected to these pins. These buffers are designed to drive capacitive loads of 100 pF or less. External buffers are necessary for driving higher load capacitances. These pins allows the user a means of instruction input and data output. With a logic **high** applied to the **BW** pin, data lines D8–D15 are placed in a high impedance state and data lines D0–D7 are used for instruction input and data output when the LM12(H)454/8 is connected to an 8-bit wide data bus. A logic **low** on the **BW** pin allows the LM12(H)454/8 to exchange information over a 16-bit wide data bus.

$\overline{RD}$ Input for the active low READ bus control signal. The data input/output TRI-STATE buffers, as selected by the logic signal applied to the **BW** pin, are enabled when $\overline{RD}$ and $\overline{CS}$ are both low. This allows the LM12(H)454/8 to transmit information onto the data bus.

$\overline{WR}$ Input for the active low WRITE bus control signal. The data input/output TRI-STATE buffers, as selected by the logic signal applied to the **BW** pin, are enabled when $\overline{WR}$ and $\overline{CS}$ are both low. This allows the LM12(H)454/8 to receive information from the data bus.

$\overline{CS}$ Input for the active low Chip Select control signal. A logic low should be applied to this pin only during a READ or WRITE access to the LM12(H)454/8. The internal clocking is halted and conversion stops while Chip Select is low. Conversion resumes when the Chip Select input signal returns high.

ALE Address Latch Enable input. It is used in systems containing a multiplexed data bus. When ALE is asserted **high**, the LM12(H)454/8 accepts information on the data bus as a valid address. A high-to-low transition will latch the address data on A0–A4 while the $\overline{CS}$ is low. Any changes on A0–A4 and $\overline{CS}$ while ALE is low will not affect the LM12(H)454/8. See *Figure 10*. When a non-multiplexed bus is used, ALE is continuously asserted **high**. See *Figure 11*.

CLK External clock input pin. The LM12(H)454/8 operates with an input clock frequency in the range of 0.05 MHz to 10.0 MHz.

A0–A4 The LM12(H)454/8's address lines. They are used to access all internal registers, Conversion FIFO, and Instruction **RAM**.

SYNC Synchronization input/output. When used as an output, it is designed to drive capacitive loads of 100 pF or less. External buffers are necessary for driving higher load capacitances. SYNC is an **input** if the Configuration register's "I/O Select" bit is **low**. A rising edge on this pin causes the internal S/H to hold the input signal. The next rising clock edge either starts a conversion or makes a comparison to a programmable limit depending on which function is requested by a programming instruction. This pin will be an **output** if "I/O Select" is set **high**. The SYNC output goes high when a conversion or a comparison is started and low when completed. (See Section 2.2). An internal reset after power is first applied to the LM12(H)454/8 automatically sets this pin as an input.

BW Bus Width input pin. This input allows the LM12(H)454/8 to interface directly with either an 8- or 16-bit data bus. A logic high sets the width to 8 bits and places D8–D15 in a high impedance state. A logic low sets the width to 16 bits.

$\overline{INT}$ Active low interrupt output. This output is designed to drive capacitive loads of 100 pF or less. External buffers are necessary for driving higher load capacitances. An interrupt signal is generated any time a non-masked interrupt condition takes place. There are eight different conditions that can cause an interrupt. Any interrupt is reset by reading the Interrupt Status register. (See Section 2.3.)

DMARQ Active high Direct Memory Access Request output. This output is designed to drive capacitive loads of 100 pF or less. External buffers are necessary for driving higher load capacitances. It goes high whenever the number of conversion results in the conversion FIFO equals a programmable value stored in the Interrupt Enable register. It returns to a logic low when the FIFO is empty.

GND LM12(H)454/8 ground connection. It should be connected to a low resistance and inductance analog ground return that connects directly to the system power supply ground.

IN0–IN7 (IN0–IN3
LM12H454
LM12454)
The eight (LM12(H)458) or four (LM12454) analog inputs. A given channel is selected through the instruction RAM. Any of the channels can be configured as an independent single-ended input. Any pair of channels, whether adjacent or non-adjacent, can operate as a fully differential pair.

S/H IN+ S/H IN–
The LM12454's non-inverting and inverting inputs to the internal S/H.

MUXOUT+ MUXOUT–
The LM12454's non-inverting and inverting outputs from the internal multiplexer.

V_{REF-} The negative reference input. The LM12(H)454/8 operate with $0V \le V_{REF-} \le V_{REF+}$. This pin should be bypassed to ground with a parallel combination of 10 µF and 0.1 µF (ceramic) capacitors.

V_{REF+} The positive reference input. The LM12(H)454/8 operate with $0V \le V_{REF+} \le V_A+$. This pin should be bypassed to ground with a parallel combination of 10 µF and 0.1 µF (ceramic) capacitors.

V_{REFOUT} The internal 2.5V bandgap's output pin. This pin should be bypassed to ground with a 100 µF capacitor.

1.0 Functional Description

The LM12454 and LM12(H)458 are multi-functional Data Acquisition Systems that include a fully differential 12-bit-plus-sign self-calibrating analog-to-digital converter (ADC) with a two's-complement output format, an 8-channel (LM12(H)458) or a 4-channel (LM12454) analog multiplexer, an internal 2.5V reference, a first-in-first-out (FIFO) register that can store 32 conversion results, and an Instruction RAM that can store as many as eight instructions to be sequentially executed. The LM12454 also has a differential multiplexer output and a differential S/H input. All of this circuitry operates on only a single +5V power supply.

The LM12(H)454/8 have three modes of operation:

12-bit + sign with correction

8-bit + sign without correction

8-bit + sign comparison mode ("watchdog" mode)

The fully differential 12-bit-plus-sign ADC uses a charge redistribution topology that includes calibration capabilities. Charge re-distribution ADCs use a capacitor ladder in place of a resistor ladder to form an internal DAC. The DAC is used by a successive approximation register to generate intermediate voltages between the voltages applied to V_{REF-} and V_{REF+}. These intermediate voltages are compared against the sampled analog input voltage as each bit is generated. The number of intermediate voltages and comparisons equals the ADC's resolution. The correction of each bit's accuracy is accomplished by calibrating the capacitor ladder used in the ADC.

Two different calibration modes are available; one compensates for offset voltage, or zero error, while the other corrects both offset error and the ADC's linearity error.

When correcting offset only, the offset error is measured once and a correction coefficient is created. During the full calibration, the offset error is measured eight times, averaged, and a correction coefficient is created. After completion of either calibration mode, the offset correction coefficient is stored in an internal offset correction register.

The LM12(H)454/8's overall linearity correction is achieved by correcting the internal DAC's capacitor mismatch. Each capacitor is compared eight times against all remaining smaller value capacitors and any errors are averaged. A correction coefficient is then created and stored in one of the thirteen internal linearity correction registers. An internal state machine, using patterns stored in an internal 16 x 8-bit ROM, executes each calibration algorithm.

Once calibrated, an internal arithmetic logic unit (ALU) uses the offset correction coefficient and the 13 linearity correction coefficients to reduce the conversion's offset error and linearity error, in the background, during the 12-bit + sign conversion. The 8-bit + sign conversion and comparison modes use only the offset coefficient. The 8-bit + sign mode performs a conversion in less than half the time used by the 12-bit + sign conversion mode.

The LM12(H)454/8's "watchdog" mode is used to monitor a single-ended or differential signal's amplitude. Each sampled signal has two limits. An interrupt can be generated if the input signal is above or below either of the two limits. This allows interrupts to be generated when analog voltage inputs are "inside the window" or, alternatively, "outside the window". After a "watchdog" mode interrupt, the processor can then request a conversion on the input signal and read the signal's magnitude.

The analog input multiplexer can be configured for any combination of single-ended or fully differential operation. Each input is referenced to ground when a multiplexer channel operates in the single-ended mode. Fully differential analog input channels are formed by pairing any two channels together.

The LM12454's multiplexer outputs and S/H inputs (MUXOUT+, MUXOUT– and S/H IN+, S/H IN–) provide the option for additional analog signal processing. Fixed-gain amplifiers, programmable-gain amplifiers, filters, and other processing circuits can operate on the signal applied to the selected multiplexer channel(s). If external processing is not used, connect MUXOUT+ to S/H IN+ and MUXOUT– to S/H IN–.

The LM12(H)454/8's internal S/H is designed to operate at its minimum acquisition time (1.13 µs, 12 bits) when the source impedance, R_S, is $\leq 60\Omega$ ($f_{CLK} \leq 8$ MHz). When $60\Omega < R_S \leq 4.17\ k\Omega$, the internal S/H's acquisition time can be increased to a maximum of 4.88 µs (12 bits, $f_{CLK} = 8$ MHz). See Section 2.1 (Instruction RAM "00") Bits 12–15 for more information.

An internal 2.5V bandgap reference output is available at pin 44. This voltage can be used as the ADC reference for ratiometric conversion or as a virtual ground for front-end analog conditioning circuits. The V_{REFOUT} pin should be bypassed to ground with a 100 µF capacitor.

Microprocessor overhead is reduced through the use of the internal conversion FIFO. Thirty-two consecutive conversions can be completed and stored in the FIFO without any microprocessor intervention. The microprocessor can, at any time, interrogate the FIFO and retrieve its contents. It can also wait for the LM12(H)454/8 to issue an interrupt when the FIFO is full or after any number (≤32) of conversions have been stored.

Conversion sequencing, internal timer interval, multiplexer configuration, and many other operations are programmed and set in the Instruction RAM.

A diagnostic mode is available that allows verification of the LM12(H)458's operation. The diagnostic mode is disabled in the LM12454. This mode internally connects the voltages present at the V_{REFOUT}, V_{REF+}, V_{REF-}, and GND pins to the internal V_{IN+} and V_{IN-} S/H inputs. This mode is activated by setting the Diagnostic bit (Bit 11) in the Configuration register to a "1". More information concerning this mode of operation can be found in Section 2.2.

2.0 Internal User-Programmable Registers

2.1 INSTRUCTION RAM

The instruction RAM holds up to eight sequentially executable instructions. Each 48-bit long instruction is divided into three 16-bit sections. READ and WRITE operations can be issued to each 16-bit section using the instruction's address and the 2-bit "RAM pointer" in the Configuration register. The eight instructions are located at addresses 0000 through 0111 (A4–A1, BW = 0) when using a 16-bit wide data bus or at addresses 00000 through 01111 (A4–A0, BW = 1) when using an 8-bit wide data bus. They can be accessed and programmed in random order.

Any Instruction RAM READ or WRITE can affect the sequencer's operation:

The Sequencer should be stopped by setting the RESET bit to a "1" or by resetting the START bit in the Configuration Register and waiting for the current instruction to finish execution before any Instruction RAM READ or WRITE is initiated. Bit 0 of the Configuration Register indicates the Sequencer Status. See paragraph 2.2 for information on the Configuration Register.

A soft RESET should be issued by writing a "1" to the Configuration Register's RESET bit after any READ or WRITE to the Instruction RAM.

The three sections in the Instruction RAM are selected by the Configuration Register's 2-bit "RAM Pointer", bits D8 and D9. The first 16-bit Instruction RAM section is selected with the RAM Pointer equal to "00". This section provides multiplexer channel selection, as well as resolution, acquisition time, etc. The second 16-bit section holds "watchdog" limit #1, its sign, and an indicator that shows that an interrupt can be generated if the input signal is greater or less than the programmed limit. The third 16-bit section holds "watchdog" limit #2, its sign, and an indicator that shows that an interrupt can be generated if the input signal is greater or less than the programmed limit.

Instruction RAM "00"

Bit 0 is the LOOP bit. It indicates the last instruction to be executed in any instruction sequence when it is set to a "1". The next instruction to be executed will be instruction 0.

Bit 1 is the PAUSE bit. This controls the Sequencer's operation. When the PAUSE bit is set ("1"), the Sequencer will stop after reading the current instruction and before executing it, and the start bit in the Configuration register is automatically reset to a "0". Setting the PAUSE also causes an interrupt to be issued. The Sequencer is restarted by placing a "1" in the Configuration register's Bit 0 (Start bit).

After the Instruction RAM has been programmed and the RESET bit is set to "1", the Sequencer retrieves Instruction 000, decodes it, and waits for a "1" to be placed in the Configuration's START bit. The START bit value of "0" "overrides" the action of Instruction 000's PAUSE bit when the Sequencer is started. Once started, the Sequencer executes Instruction 000 and retrieves, decodes, and executes each of the remaining instructions. No PAUSE Interrupt (INT 5) is generated the first time the Sequencer executes Instruction 000 having a PAUSE bit set to "1". When the Sequencer encounters a LOOP bit or completes all eight instructions, Instruction 000 is retrieved and decoded. A set PAUSE bit in Instruction 000 now halts the Sequencer before the instruction is executed.

Bits 2–4 select which of the eight input channels ("000" to "111" for IN0–IN7) will be configured as non-inverting inputs to the LM12(H)458's ADC. (See *Table 1*.) They select which of the four input channels ("000" to "011" for IN0–IN4) will be configured as non-inverting inputs to the LM12454's ADC. (See *Table 2*.)

Bits 5–7 select which of the seven input channels ("001" to "111" for IN1 to IN7) will be configured as inverting inputs to the LM12(H)458's ADC. (See *Table 1*.) They select which of the three input channels ("001" to "011" for IN1–IN4) will be configured as inverting inputs to the LM12454's ADC. (See *Table 2*.) Fully differential operation is created by selecting two multiplexer channels, one operating in the non-inverting mode and the other operating in the inverting mode. A code of "000" selects ground as the inverting input for single ended operation.

Bit 8 is the SYNC bit. Setting Bit 8 to "1" causes the Sequencer to suspend operation at the end of the internal S/H's acquisition cycle and to wait until a rising edge appears at the SYNC pin. When a rising edge appears, the S/H acquires the input signal magnitude and the ADC performs a conversion on the clock's next rising edge. When the SYNC pin is used as an input, the Configuration register's "I/O Select" bit (Bit 7) must be set to a "0". With SYNC configured as an input, it is possible to synchronize the start of a conversion to an external event. This is useful in applications such as digital signal processing (DSP) where the exact timing of conversions is important.

When the LM12(H)454/8 are used in the "watchdog" mode with external synchronization, two rising edges on the SYNC input are required to initiate two comparisons. The first rising edge initiates the comparison of the selected analog input signal with Limit #1 (found in Instruction RAM "01") and the second rising edge initiates the comparison of the same analog input signal with Limit #2 (found in Instruction RAM "10").

Bit 9 is the TIMER bit. When Bit 9 is set to "1", the Sequencer will halt until the internal 16-bit Timer counts down to zero. During this time interval, no "watchdog" comparisons or analog-to-digital conversions will be performed.

Bit 10 selects the ADC conversion resolution. Setting Bit 10 to "1" selects 8-bit + sign and when reset to "0" selects 12-bit + sign.

Bit 11 is the "watchdog" comparison mode enable bit. When operating in the "watchdog" comparison mode, the selected analog input signal is compared with the programmable values stored in Limit #1 and Limit #2 (see Instruction RAM "01" and Instruction RAM "10"). Setting Bit 11 to "1" causes two comparisons of the selected analog input signal with the two stored limits. When Bit 11 is reset to "0", an 8-bit + sign or 12-bit + sign (depending on the state of Bit 10 of Instruction RAM "00") conversion of the input signal can take place.

A4	A3	A2	A1	Purpose	Type	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0 to 1	0 to 1	0 to 1	Instruction RAM (RAM Pointer = 00)	R/W	Acquisition Time				Watch-dog	8/$\overline{12}$	Timer	Sync	V_{IN-} (MUXOUT−) (Note 19)			V_{IN+} (MUXOUT+) (Note 19)			Pause	Loop
0	0 to 1	0 to 1	0 to 1	Instruction RAM (RAM Pointer = 01)	R/W	Don't Care						>/$\overline{<}$	Sign	Limit #1							
0	0 to 1	0 to 1	0 to 1	Instruction RAM (RAM Pointer = 10)	R/W	Don't Care						>/$\overline{<}$	Sign	Limit #2							
1	0	0	0	Configuration Register	R/W	Don't Care				DIAG * (Note 20)	Test = 0	RAM Pointer		i/O Sel	Auto $Zero_{ec}$	Char Mask	Stand-by	Full CAL	Auto-Zero	Reset	Start
1	0	0	1	Interrupt Enable Register	R/W	Number of Conversions in Conversion FIFO to Generate INT2					Sequencer Address to Generate INT1			INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0
1	0	1	0	Interrupt Status Register	R	Actual Number of Conversion Results in Conversion FIFO					Address of Sequencer Instruction being Executed			INST7	INST6	INST5	INST4	INST3	INST2	INST1	INST0
1	0	1	1	Timer Register	R/W	Timer Preset High Byte								Timer Preset Low Byte							
1	1	0	0	Conversion FIFO	R	Address or Sign			Sign	Conversion Data: MSBs				Conversion Data: LSBs							
1	1	0	1	Limit Status Register	R	Limit #2: Status								Limit #1: Status							

Note 19: LM12454 (Refer to *Table 2*).

Note 20: LM12(H)458 only. Must be set to "0" for the LM12454.

FIGURE 13. LM12(H)454/8 Memory Map for 16-Bit Wide Data Bus (BW = "0", Test Bit = "0" and A0 = Don't Care)

2.0 Internal User-Programmable Registers (Continued)

A4	A3	A2	A1	A0	Purpose	Type	D7	D6	D5	D4	D3	D2	D1	D0
0	0 to 1	0 to 1	0 to 1	0	Instruction RAM (RAM Pointer = 00)	R/W	V_{IN-} (MUXOUT−) (Note 21)			V_{IN+} (MUXOUT+) (Note 21)			Pause	Loop
0	0 to 1	0 to 1	0 to 1	1		R/W	Acquisition Time				Watch-dog	8/12	Timer	Sync
0	0 to 1	0 to 1	0 to 1	0	Instruction RAM (RAM Pointer = 01)	R/W	Comparison Limit #1							
						R/W	Don't Care						>/<	Sign
0	0 to 1	0 to 1	0 to 1	1		R/W	Don't Care						>/<	Sign
0	0 to 1	0 to 1	0 to 1	0	Instruction RAM (RAM Pointer = 10)	R/W	Comparison Limit #2							
0	0 to 1	0 to 1	0 to 1	1		R/W	Don't Care						>/<	Sign
1	0	0	0	0	Configuration Register	R/W	I/O Sel	Auto $Zero_{ec}$	Chan Mask	Stand-by	Full Cal	Auto-Zero	Reset	Start
1	0	0	0	1		R/W	Don't Care				DIAG (Note 22)	Test = 0	RAM Pointer	
1	0	0	1	0	Interrupt Enable Register	R/W	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0
1	0	0	1	1		R/W	Number of Conversions in Conversion FIFO to Generate INT2					Sequencer Address to Generate INT1		
1	0	1	0	0	Interrupt Status Register	R	INST7	INST6	INST5	INST4	INST3	INST2	INST1	INST0
1	0	1	0	1		R	Actual Number of Conversions Results in Conversion FIFO					Address of Sequencer Instruction being Executed		
1	0	1	1	0	Timer Register	R/W	Timer Preset: Low Byte							
1	0	1	1	1		R/W	Timer Preset: High Byte							
1	1	0	0	0	Conversion FIFO	R	Conversion Data: LSBs							
1	1	0	0	1		R	Address or Sign			Sign	Conversion Data: MSBs			
1	1	0	1	0	Limit Status Register	R	Limit #1 Status							
1	1	0	1	1		R	Limit #2 Status							

FIGURE 14. LM12(H)454/8 Memory Map for 8-Bit Wide Data Bus (BW = "1" and Test Bit = "0")

Note 21: LM12454 (Refer to *Table 2*).

Note 22: LM12(H)458 only. Must be set to "0" for the LM12454.

2.0 Internal User-Programmable Registers (Continued)

Bits 12–15 are used to store the user-programmable acquisition time. The Sequencer keeps the internal S/H in the acquisition mode for a fixed number of clock cycles (nine clock cycles, for 12-bit + sign conversions and two clock cycles for 8-bit + sign conversions or "watchdog" comparisons) plus a variable number of clock cycles equal to twice the value stored in Bits 12–15. Thus, the S/H's acquisition time is (9 + 2D) clock cycles for 12-bit + sign conversions and (2 + 2D) clock cycles for 8-bit + sign conversions or "watchdog" comparisons, where D is the value stored in Bits 12–15. The minimum acquisition time compensates for the typical internal multiplexer series resistance of 2 kΩ, and any additional delay created by Bits 12–15 compensates for source resistances greater than 60Ω (100Ω). (For this acquisition time discussion, numbers in ( ) are shown for the LM12(H)454/8 operating at 5 MHz.) The necessary acquisition time is determined by the source impedance at the multiplexer input. If the source resistance (R_S) < 60Ω (100Ω) and the clock frequency is 8 MHz, the value stored in bits 12–15 (D) can be 0000. If R_S > 60Ω (100Ω), the following equations determine the value that should be stored in bits 12–15.

$$D = 0.45 \times R_S \times f_{CLK}$$

for 12-bits + sign

$$D = 0.36 \times R_S \times f_{CLK}$$

for 8-bits + sign and "watchdog"

R_S is in kΩ and f_{CLK} is in MHz. Round the result to the next higher integer value. If D is greater than 15, it is advisable to lower the source impedance by using an analog buffer between the signal source and the LM12(H)458's multiplexer inputs. The value of D can also be used to compensate for the settling or response time of external processing circuits connected between the LM12454's MUXOUT and S/H IN pins.

Instruction RAM "01"

The second Instruction RAM section is selected by placing a "01" in Bits 8 and 9 of the Configuration register.

Bits 0–7 hold "watchdog" **limit #1**. When Bit 11 of Instruction RAM "00" is set to a "1", the LM12(H)454/8 performs a "watchdog" comparison of the sampled analog input signal with the limit #1 value first, followed by a comparison of the same sampled analog input signal with the value found in limit #2 (Instruction RAM "10").

Bit 8 holds limit #1's sign.

Bit 9's state determines the limit condition that generates a "watchdog" interrupt. A "1" causes a voltage greater than limit #1 to generate an interrupt, while a "0" causes a voltage less than limit #1 to generate an interrupt.

Bits 10–15 are not used.

Instruction RAM "10"

The third Instruction RAM section is selected by placing a "10" in Bits 8 and 9 of the Configuration register.

Bits 0–7 hold "watchdog" **limit #2**. When Bit 11 of Instruction RAM "00" is set to a "1", the LM12(H)454/8 performs a "watchdog" comparison of the sampled analog input signal with the limit #1 value first (Instruction RAM "01"), followed by a comparison of the same sampled analog input signal with the value found in limit #2.

Bit 8 holds limit #2's sign.

Bit 9 's state determines the limit condition that generates a "watchdog" interrupt. A "1" causes a voltage greater than limit #2 to generate an interrupt, while a "0" causes a voltage less than limit #2 to generate an interrupt.

Bits 10–15 are not used.

2.2 CONFIGURATION REGISTER

The Configuration register, 1000 (A4–A1, BW = 0) or 1000x (A4–A0, BW = 1) is a 16-bit control register with read/write capability. It acts as the LM12454's and LM12(H)458's "control panel" holding global information as well as start/stop, reset, self-calibration, and stand-by commands.

Bit 0 is the START/STOP bit. Reading Bit 0 returns an indication of the Sequencer's status. A "0" indicates that the Sequencer is stopped and waiting to execute the next instruction. A "1" shows that the Sequencer is running. Writing a "0" halts the Sequencer when the current instruction has finished execution. The next instruction to be executed is pointed to by the instruction pointer found in the status register. A "1" restarts the Sequencer with the instruction currently pointed to by the instruction pointer. (See Bits 8–10 in the Interrupt Status register.)

Bit 1 is the LM12(H)454/8's system RESET bit. Writing a "1" to Bit 1 stops the Sequencer (resetting the Configuration register's START/STOP bit), resets the Instruction pointer to "000" (found in the Interrupt Status register), clears the Conversion FIFO, and resets all interrupt flags. The RESET bit will return to "0" after two clock cycles unless it is forced high by writing a "1" into the Configuration register's Standby bit. A reset signal is internally generated when power is first applied to the part. No operation should be started until the RESET bit is "0".

Writing a "1" to **Bit 2** initiates an auto-zero offset voltage calibration. Unlike the eight-sample auto-zero calibration performed during the full calibration procedure, Bit 2 initiates a "short" auto-zero by sampling the offset once and creating a correction coefficient (full calibration averages eight samples of the converter offset voltage when creating a correction coefficient). If the Sequencer is running when Bit 2 is set to "1", an auto-zero starts immediately after the conclusion of the currently running instruction. Bit 2 is reset automatically to a "0" and an interrupt flag (Bit 3, in the Interrupt Status register) is set at the end of the auto-zero (76 clock cycles). After completion of an auto-zero calibration, the Sequencer fetches the next instruction as pointed to by the Instruction RAM's pointer and resumes execution. If the Sequencer is stopped, an auto-zero is performed immediately at the time requested.

Writing a "1" to **Bit 3** initiates a complete calibration process that includes a "long" auto-zero offset voltage correction (this calibration averages eight samples of the comparator offset voltage when creating a correction coefficient) followed by an ADC linearity calibration. This complete calibration is started after the currently running instruction is completed if the Sequencer is running when Bit 3 is set to "1". Bit 3 is reset automatically to a "0" and an interrupt flag (Bit 4, in the Interrupt Status register) will be generated at the end of the calibration procedure (4944 clock cycles). After completion of a full auto-zero and linearity calibration, the Sequencer fetches the next instruction as pointed to by the Instruction RAM's pointer and resumes execution. If the Sequencer is stopped, a full calibration is performed immediately at the time requested.

Bit 4 is the Standby bit. Writing a "1" to Bit 4 immediately places the LM12(H)454/8 in Standby mode. Normal operation returns when Bit 4 is reset to a "0". The Standby com-

2.0 Internal User-Programmable Registers (Continued)

mand ("1") disconnects the external clock from the internal circuitry, decreases the LM12(H)454/8's internal analog circuitry power supply current, and preserves all internal RAM contents. After writing a "0" to the Standby bit, the LM12(H)454/8 returns to an operating state identical to that caused by exercising the RESET bit. A Standby completion interrupt is issued after a power-up completion delay that allows the analog circuitry to settle. The Sequencer should be restarted only after the Standby completion is issued. The Instruction RAM can still be accessed through read and write operations while the LM12(H)454/8 are in Standby Mode.

Bit 5 is the Channel Address Mask. If Bit 5 is set to a "1", Bits 13–15 in the conversion FIFO will be equal to the sign bit (Bit 12) of the conversion data. Resetting Bit 5 to a "0" causes conversion data Bits 13 through 15 to hold the instruction pointer value of the instruction to which the conversion data belongs.

Bit 6 is used to select a "short" auto-zero correction for every conversion. The Sequencer automatically inserts an auto-zero before every conversion or "watchdog" comparison if Bit 6 is set to "1". No automatic correction will be performed if Bit 6 is reset to "0".

The LM12(H)454/8's offset voltage, after calibration, has a typical drift of 0.1 LSB over a temperature range of −40˚C to +85˚C. This small drift is less than the variability of the change in offset that can occur when using the auto-zero correction with each conversion. This variability is the result of using only one sample of the offset voltage to create a correction value. This variability decreases when using the full calibration mode because eight samples of the offset voltage are taken, averaged, and used to create a correction value.

Bit 7 is used to program the SYNC pin (29) to operate as either an input or an output. The SYNC pin becomes an output when Bit 7 is a "1" and an input when Bit 7 is a "0". With SYNC programmed as an input, the rising edge of any logic signal applied to pin 29 will start a conversion or "watchdog" comparison. Programmed as an output, the logic level at pin 29 will go high at the start of a conversion or "watchdog" comparison and remain high until either have finished. See Instruction RAM "00", Bit 8.

Bits 8 and **9** form the RAM Pointer that is used to select each of a 48-bit instruction's three 16-bit sections during read or write actions. A "00" selects Instruction RAM section one, "01" selects section two, and "10" selects section three.

Bit 10 activates the Test mode that is used only during production testing. Leave this bit reset to "0".

Bit 11 is the Diagnostic bit and is available only in the LM12(H)458. It can be activated by setting it to a "1" (the Test bit must be reset to a "0"). The Diagnostic mode, along with a correctly chosen instruction, allows verification that the LM12(H)458's ADC is performing correctly. When activated, the inverting and non-inverting inputs are connected as shown in *Table 1*. As an example, an instruction with "001" for both V_{IN+} and V_{IN-} while using the Diagnostic mode typically results in a full-scale output.

2.3 INTERRUPTS

The LM12454 and LM12(H)458 have eight possible interrupts, all with the same priority. Any of these interrupts will cause a hardware interrupt to appear on the $\overline{INT}$ pin (31) if they are not masked (by the Interrupt Enable register). The Interrupt Status register is then read to determine which of the eight interrupts has been issued.

TABLE 1. LM12(H)458 Input Multiplexer Channel Configuration Showing Normal Mode and Diagnostic Mode

Channel Selection Data	Normal Mode		Diagnostic Mode	
	V_{IN+}	V_{IN-}	V_{IN+}	V_{IN-}
000	IN0	GND	V_{REFOUT}	GND
001	IN1	IN1	V_{REF+}	V_{REF-}
010	IN2	IN2	IN2	IN2
011	IN3	IN3	IN3	IN3
100	IN4	IN4	IN4	IN4
101	IN5	IN5	IN5	IN5
110	IN6	IN6	IN6	IN6
111	IN7	IN7	IN7	IN7

TABLE 2. LM12454 Input Multiplexer Channel Configuration

Channel Selection Data	MUX+	MUX−
000	IN0	GND
001	IN1	IN1
010	IN2	IN2
011	IN3	IN3
1XX	OPEN	OPEN

NOTE: The LM12(H)454 is no longer available. Information shown for reference only.

The Interrupt Status register, 1010 (A4–A1, BW = 0) or 1010x (A4–A0, BW = 1) must be cleared by reading it after writing to the Interrupt Enable register. This removes any spurious interrupts on the $\overline{INT}$ pin generated during an Interrupt Enable register access.

Interrupt 0 is generated whenever the analog input voltage on a selected multiplexer channel crosses a limit while the LM12(H)454/8 are operating in the "watchdog" comparison mode. Two sequential comparisons are made when the LM12(H)454/8 are executing a "watchdog" instruction. Depending on the logic state of Bit 9 in the Instruction RAM's second and third sections, an interrupt will be generated either when the input signal's magnitude is greater than or less than the programmable limits. (See the Instruction RAM, Bit 9 description.) The Limit Status register will indicate which preprogrammed limit, #1 or #2 and which instruction was executing when the limit was crossed.

Interrupt 1 is generated when the Sequencer reaches the instruction counter value specified in the Interrupt Enable register's bits 8–10. This flag appears before the instruction's execution.

Interrupt 2 is activated when the Conversion FIFO holds a number of conversions equal to the programmable value stored in the Interrupt Enable register's Bits 11–15. This value ranges from 0001 to 1111, representing 1 to 31 conversions stored in the FIFO. A user-programmed value of 0000 has no meaning. See Section 3.0 for more FIFO information.

2.0 Internal User-Programmable Registers (Continued)

The completion of the short, single-sample auto-zero calibration generates **Interrupt 3**.

The completion of a full auto-zero and linearity self-calibration generates **Interrupt 4**.

Interrupt 5 is generated when the Sequencer encounters an instruction that has its Pause bit (Bit 1 in Instruction RAM "00") set to "1".

The LM12(H)454/8 issues **Interrupt 6** whenever it senses that its power supply voltage is dropping below 4V (typ). This interrupt indicates the potential corruption of data returned by the LM12(H)454/8.

Interrupt 7 is issued after a short delay (10 ms typ) while the LM12(H)454/8 returns from Standby mode to active operation using the Configuration register's Bit 4. This short delay allows the internal analog circuitry to settle sufficiently, ensuring accurate conversion results.

2.4 INTERRUPT ENABLE REGISTER

The Interrupt Enable register at address location 1001 (A4–A1, BW = 0) or 1001x (A4–A0, BW = 1) has READ/WRITE capability. An individual interrupt's ability to produce an external interrupt at pin 31 ($\overline{INT}$) is accomplished by placing a "1" in the appropriate bit location. Any of the internal interrupt-producing operations will set their corresponding bits to "1" in the Interrupt Status register regardless of the state of the associated bit in the Interrupt Enable register. See Section 2.3 for more information about each of the eight internal interrupts.

Bit 0 enables an external interrupt when an internal "watchdog" comparison limit interrupt has taken place.

Bit 1 enables an external interrupt when the Sequencer has reached the address stored in Bits 8–10 of the Interrupt Enable register.

Bit 2 enables an external interrupt when the Conversion FIFO's limit, stored in Bits 11–15 of the Interrupt Enable register, has been reached.

Bit 3 enables an external interrupt when the single-sample auto-zero calibration has been completed.

Bit 4 enables an external interrupt when a full auto-zero and linearity self-calibration has been completed.

Bit 5 enables an external interrupt when an internal Pause interrupt has been generated.

Bit 6 enables an external interrupt when a low power supply condition ($V_A+ < 4V$) has generated an internal interrupt.

Bit 7 enables an external interrupt when the LM12(H)454/8 return from power-down to active mode.

Bits 8 – 10 form the storage location of the user-programmable value against which the Sequencer's address is compared. When the Sequencer reaches an address that is equal to the value stored in Bits 8–10, an internal interrupt is generated and appears in Bit 1 of the Interrupt Status register. If Bit 1 of the Interrupt Enable register is set to "1", an external interrupt will appear at pin 31 ($\overline{INT}$).

The value stored in bits 8–10 ranges from 000 to 111, representing 0 to 7 instructions stored in the Instruction RAM. After the Instruction RAM has been programmed and the RESET bit is set to "1", the Sequencer is started by placing a "1" in the Configuration register's START bit. Setting the INT 1 trigger value to 000 **does not generate** an INT 1 the **first** time the Sequencer retrieves and decodes Instruction 000. The Sequencer **generates** INT 1 (by placing a "1" in the Interrupt Status register's Bit 1) the **second time and after** the Sequencer encounters Instruction 000. It is important to remember that the Sequencer continues to operate even if an Instruction interrupt (INT 1) is internally or externally generated. The only mechanisms that stop the Sequencer are an instruction with the PAUSE bit set to "1" (halts before instruction execution), placing a "0" in the Configuration register's START bit, or placing a "1" in the Configuration register's RESET bit.

Bits 11–15 hold the number of conversions that must be stored in the Conversion FIFO in order to generate an internal interrupt. This internal interrupt appears in Bit 2 of the Interrupt Status register. If Bit 2 of the Interrupt Enable register is set to "1", an external interrupt will appear at pin 31 (INT).

3.0 Other Registers and Functions

3.1 INTERRUPT STATUS REGISTER

This read-only register is located at address 1010 (A4–A1, BW = 0) or 1010x (A4–A0, BW = 1). The corresponding flag in the Interrupt Status register goes high ("1") any time that an interrupt condition takes place, whether an interrupt is enabled or disabled in the Interrupt Enable register. Any of the active ("1") Interrupt Status register flags are reset to "0" whenever this register is read or a device reset is issued (see Bit 1 in the Configuration Register).

Bit 0 is set to "1" when a "watchdog" comparison limit interrupt has taken place.

Bit 1 is set to "1" when the Sequencer has reached the address stored in Bits 8–10 of the Interrupt Enable register.

Bit 2 is set to "1" when the Conversion FIFO's limit, stored in Bits 11–15 of the Interrupt Enable register, has been reached.

Bit 3 is set to "1" when the single-sample auto-zero has been completed.

Bit 4 is set to "1" when an auto-zero and full linearity self-calibration has been completed.

Bit 5 is set to "1" when a Pause interrupt has been generated.

Bit 6 is set to "1" when a low-supply voltage condition ($V_A+ < 4V$) has taken place.

Bit 7 is set to "1" when the LM12(H)454/8 return from power-down to active mode.

Bits 8–10 hold the Sequencer's actual instruction address while it is running.

Bits 11–15 hold the actual number of conversions stored in the Conversion FIFO while the Sequencer is running.

3.2 LIMIT STATUS REGISTER

The read-only register is located at address 1101 (A4–A1, BW = 0) or 1101x (A4–A0, BW = 1). This register is used in tandem with the Limit #1 and Limit #2 registers in the Instruction RAM. Whenever a given instruction's input voltage exceeds the limit set in its corresponding Limit register (#1 or #2), a bit, corresponding to the instruction number, is set in the Limit Status register. Any of the active ("1") Limit Status flags are reset to "0" whenever this register is read or a device reset is issued (see Bit 1 in the Configuration register). This register holds the status of limits #1 and #2 for each of the eight instructions.

Bits 0–7 show the Limit #1 status. Each bit will be set high ("1") when the corresponding instruction's input voltage ex-

3.0 Other Registers and Functions

(Continued)

ceeds the threshold stored in the instruction's Limit #1 register. When, for example, instruction 3 is a "watchdog" operation (Bit 11 is set high) and the input for instruction 3 meets the magnitude and/or polarity data stored in instruction 3's Limit #1 register, Bit 3 in the Limit Status register will be set to a "1".

Bits 8–15 show the Limit #2 status. Each bit will be set high ("1") when the corresponding instruction's input voltage exceeds the threshold stored in the instruction's Limit #2 register. When, for example, the input to instruction 6 meets the value stored in instruction 6's Limit #2 register, Bit 14 in the Limit Status register will be set to a "1".

3.3 TIMER

The LM12(H)454/8 have an on-board 16-bit timer that includes a 5-bit pre-scaler. It uses the clock signal applied to pin 23 as its input. It can generate time intervals of 0 through 2^{21} clock cycles in steps of 2^5. This time interval can be used to delay the execution of instructions. It can also be used to slow the conversion rate when converting slowly changing signals. This can reduce the amount of redundant data stored in the FIFO and retrieved by the controller.

The user-defined timing value used by the Timer is stored in the 16-bit READ/WRITE Timer register at location 1011 (A4–A1, BW = 0) or 1011x (A4–A0, BW = 1) and is preloaded automatically. Bits 0–7 hold the preset value's low byte and Bits 8–15 hold the high byte. The Timer is activated by the Sequencer only if the current instruction's Bit 9 is set ("1"). If the equivalent decimal value "N" ($0 \le N \le 2^{16} - 1$) is written inside the 16-bit Timer register and the Timer is enabled by setting an instruction's bit 9 to a "1", the Sequencer will delay the same instruction's execution by halting at state 3 (S3), as shown in *Figure 15*, for 32 x N + 2 clock cycles.

3.4 DMA

The DMA works in tandem with Interrupt 2. An active DMA Request on pin 32 (DMARQ) requires that the FIFO interrupt be enabled. The voltage on the DMARQ pin goes high when the number of conversions in the FIFO equals the 5-bit value stored in the Interrupt Enable register (bits 11–15). The voltage on the $\overline{\text{INT}}$ pin goes low at the same time as the voltage on the DMARQ pin goes high. The voltage on the DMARQ pin goes low when the FIFO is emptied. The Interrupt Status register must be read to clear the FIFO interrupt flag in order to enable the next DMA request.

DMA operation is optimized through the use of the 16-bit data bus connection (a logic "0" applied to the BW pin). Using this bus width allows DMA controllers that have single address Read/Write capability to easily unload the FIFO. Using DMA on an 8-bit data bus is more difficult. Two read operations (low byte, high byte) are needed to retrieve each conversion result from the FIFO. Therefore, the DMA controller must be able to repeatedly access two constant addresses when transferring data from the LM12(H)454/8 to the host system.

4.0 FIFO

The result of each conversion stored in an internal read-only FIFO (First-In, First-Out) register. It is located at 1100 (A4–A1, BW = 0) or 1100x (A4–A0, BW = 1). This register has 32 16-bit wide locations. Each location holds 13-bit data. Bits 0–3 hold the four LSB's in the 12 bits + sign mode or "1110" in the 8 bits + sign mode. Bits 4–11 hold the eight MSB's and Bit 12 holds the sign bit. Bits 13–15 can hold either the sign bit, extending the register's two's complement data format to a full sixteen bits or the instruction address that generated the conversion and the resulting data. These modes are selected according to the logic state of the Configuration register's Bit 5.

The FIFO status should be read in the Interrupt Status register (Bits 11–15) to determine the number of conversion results that are held in the FIFO before retrieving them. This will help prevent conversion data corruption that may take place if the number of reads are greater than the number of conversion results contained in the FIFO. Trying to read the FIFO when it is empty may corrupt new data being written into the FIFO. Writing more than 32 conversion data into the FIFO by the ADC results in loss of the first conversion data. Therefore, to prevent data loss, it is recommended that the LM12(H)454/8's interrupt capability be used to inform the system controller that the FIFO is full.

The lower portion (A0 = 0) of the data word (Bits 0–7) should be read first followed by a read of the upper portion (A0 = 1) when using the 8-bit bus width (BW = 1). Reading the upper portion first causes the data to shift down, which results in loss of the lower byte.

Bits 0–12 hold 12-bit + sign conversion data. **Bits 0–3** will be 1110 (LSB) when using 8-bit plus sign resolution.

Bits 13–15 hold either the instruction responsible for the associated conversion data or the sign bit. Either mode is selected with Bit 5 in the Configuration register.

Using the FIFO's full depth is achieved as follows. Set the value of the Interrupt Enable register's Bits 11–15 to 11111 and the Interrupt Enable register's Bit 2 to a "1". This generates an external interrupt when the 31st conversion is stored in the FIFO. This gives the host processor a chance to send a "0" to the LM12(H)454/8's Start bit (Configuration register) and halt the ADC before it completes the 32nd conversion. The Sequencer halts after the current (32) conversion is completed. The conversion data is then transferred to the FIFO and occupies the 32nd location. FIFO overflow is avoided if the Sequencer is halted before the start of the 32nd conversion by placing a "0" in the Start bit (Configuration register). It is important to remember that the Sequencer **continues to operate even if a FIFO interrupt (INT 2) is internally or externally generated**. The only mechanisms that stop the Sequencer are an instruction with the PAUSE bit set to "1" (halts before instruction execution), placing a "0" in the Configuration register's START bit, or placing a "1" in the Configuration register's RESET bit.

5.0 Sequencer

The Sequencer uses a 3-bit counter (Instruction Pointer, or IP, in *Figure 9*) to retrieve the programmable conversion instructions stored in the Instruction RAM. The 3-bit counter is reset to 000 during chip reset or if the current executed instruction has its Loop bit (Bit 1 in any Instruction RAM "00") set high ("1"). It increments at the end of the currently executed instruction and points to the next instruction. It will continue to increment up to 111 unless an instruction's Loop bit is set. If this bit is set, the counter resets to "000" and execution begins again with the first instruction. If all instructions have their Loop bit reset to "0", the Sequencer will execute all eight instructions continuously. Therefore, it is important to realize that if less than eight instructions are programmed, the Loop bit on the last instruction must be set.

5.0 Sequencer (Continued)

Leaving this bit reset to "0" allows the Sequencer to execute "unprogrammed" instructions, the results of which may be unpredictable.

The Sequencer's Instruction Pointer value is readable at any time and is found in the Status register at Bits 8–10. The Sequencer can go through eight states during instruction execution:

State 0: The current instruction's first 16 bits are read from the Instruction RAM "00". This state is one clock cycle long.

State 1: Checks the state of the Calibration and Start bits. This is the "rest" state whenever the Sequencer is stopped using the reset, a Pause command, or the Start bit is reset low ("0"). When the Start bit is set to a "1", this state is one clock cycle long.

State 2: Perform calibration. If bit 2 or bit 6 of the Configuration register is set to a "1", state 2 is 76 clock cycles long. If the Configuration register's bit 3 is set to a "1", state 2 is 4944 clock cycles long.

State 3: Run the internal 16-bit Timer. The number of clock cycles for this state varies according to the value stored in the Timer register. The number of clock cycles is found by using the expression below

$$32T + 2$$

where $0 \leq T \leq 2^{16} - 1$.

State 7: Run the acquisition delay and read Limit #1's value if needed. The number of clock cycles for 12-bit + sign mode varies according to

$$9 + 2D$$

where D is the user-programmable 4-bit value stored in bits 12–15 of Instruction RAM "00" and is limited to $0 \leq D \leq 15$.

The number of clock cycles for 8-bit + sign or "watchdog" mode varies according to

$$2 + 2D$$

where D is the user-programmable 4-bit value stored in bits 12–15 of Instruction RAM "00" and is limited to $0 \leq D \leq 15$.

State 6: Perform first comparison. This state is 5 clock cycles long.

State 4: Read Limit #2. This state is 1 clock cycle long.

State 5: Perform a conversion or second comparison. This state takes 44 clock cycles when using the 12-bit + sign mode or 21 clock cycles when using the 8-bit + sign mode. The "watchdog" mode takes 5 clock cycles.

5.0 Sequencer (Continued)

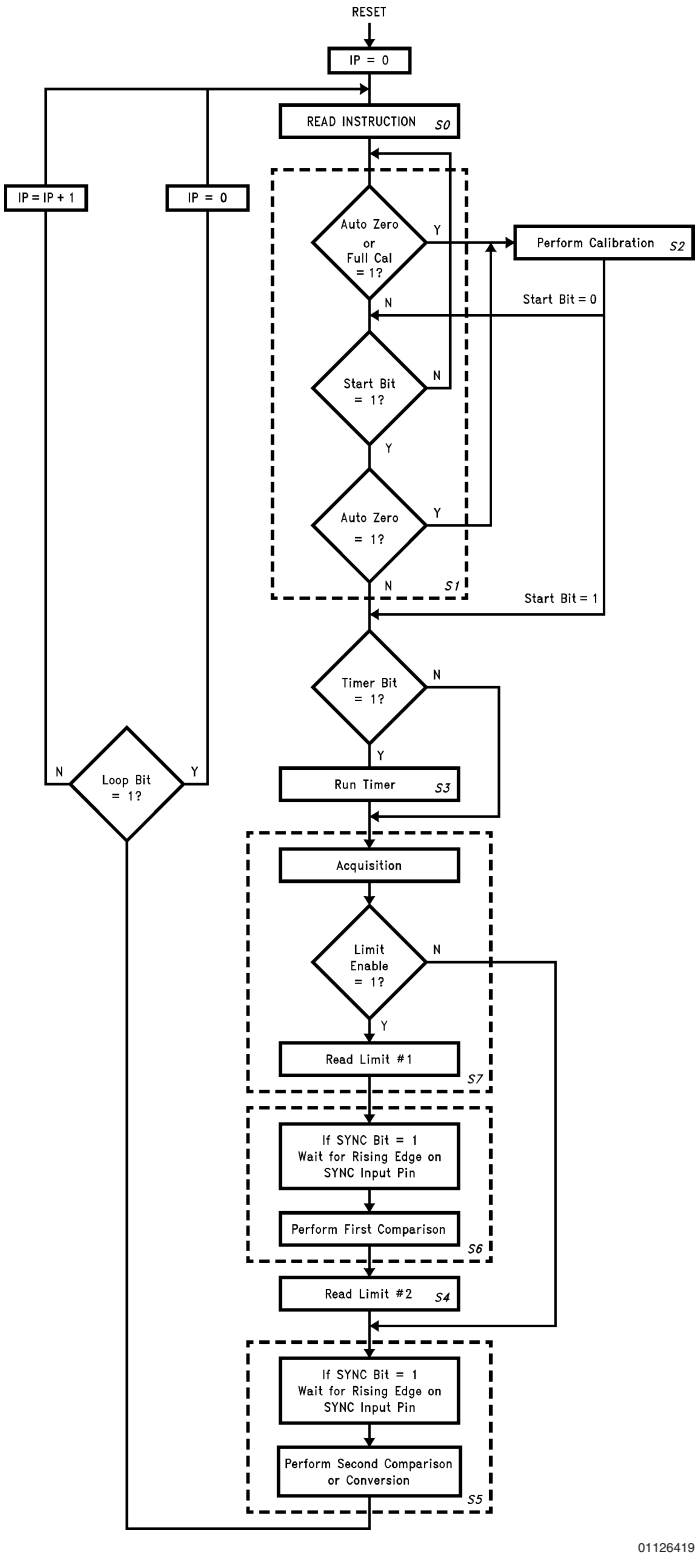


FIGURE 15. Sequencer Logic Flow Chart (IP = Instruction Pointer)

6.0 Design Considerations

6.1 REFERENCE VOLTAGE

The difference in the voltages applied to the V_{REF+} and V_{REF-} defines the analog input voltage span (the difference between the voltages applied between two multiplexer inputs or the voltage applied to one of the multiplexer inputs and analog ground), over which 4095 positive and 4096 negative codes exist. The voltage sources driving V_{REF+} or V_{REF-} must have very low output impedance and noise.

The ADC can be used in either ratiometric or absolute reference applications. In ratiometric systems, the analog input voltage is proportional to the voltage used for the ADC's reference voltage. When this voltage is the system power supply, the V_{REF+} pin is connected to V_A+ and V_{REF-} is connected to GND. This technique relaxes the system reference stability requirements because the analog input voltage and the ADC reference voltage move together. This maintains the same output code for given input conditions.

For absolute accuracy, where the analog input voltage varies between very specific voltage limits, a time and temperature stable voltage source can be connected to the reference inputs. Typically, the reference voltage's magnitude will require an initial adjustment to null reference voltage induced full-scale errors.

When using the LM12(H)454/8's internal 2.5V bandgap reference, a parallel combination of a 100 µF capacitor and a 0.1 µF capacitor connected to the V_{REFOUT} pin is recommended for low noise operation. When left unconnected, the reference remains stable without a bypass capacitor. However, ensure that stray capacitance at the V_{REFOUT} pin remains below 50 pF.

6.2 INPUT RANGE

The LM12(H)454/8's fully differential ADC and reference voltage inputs generate a two's-complement output that is found by using the equation below.

$$\text{output code} = \frac{V_{IN+} - V_{IN-}}{V_{REF+} - V_{REF-}} (4096) - \tfrac{1}{2} \qquad \text{(12-bit)}$$

$$\text{output code} = \frac{V_{IN+} - V_{IN-}}{V_{REF+} - V_{REF-}} (256) - \tfrac{1}{2} \qquad \text{(8-bit)}$$

Round up to the next integer value between –4096 to 4095 for 12-bit resolution and between –256 to 255 for 8-bit resolution if the result of the above equation is not a whole number. As an example, V_{REF+} = 2.5V, V_{REF-} = 1V, V_{IN+} = 1.5V and V_{IN-} = GND. The 12-bit + sign output code is positive full-scale, or 0,1111,1111,1111. If V_{REF+} = 5V, V_{REF-} = 1V, V_{IN+} = 3V, and V_{IN-} = GND, the 12-bit + sign output code is 0,1100,0000,0000.

6.3 INPUT CURRENT

A charging current flows into or out of (depending on the input voltage polarity) the analog input pins, IN0–IN7 at the start of the analog input acquisition time (t_{ACQ}). This current's peak value will depend on the actual input voltage applied. This charging current causes voltage spikes at the inputs. This voltage spikes will not corrupt the conversion results.

6.4 INPUT SOURCE RESISTANCE

For low impedance voltage sources (<100Ω for 5 MHz operation and <60Ω for 8 MHz operation), the input charging current will decay, before the end of the S/H's acquisition time, to a value that will not introduce any conversion errors. For higher source impedances, the S/H's acquisition time can be increased. As an example, operating with a 5 MHz clock frequency and maximum acquisition time, the LM12(H)454/8's analog inputs can handle source impedance as high as 6.67 kΩ. When operating at 8 MHz and maximum acquisition time, the LM12H454/8's analog inputs can handle source impedance as high as 4.17 kΩ. Refer to Section 2.1, Instruction RAM "00", Bits 12–15 for further information.

6.5 INPUT BYPASS CAPACITANCE

External capacitors (0.01 µF to 0.1 µF) can be connected between the analog input pins, IN0–IN7, and analog ground to filter any noise caused by inductive pickup associated with long input leads. It will not degrade the conversion accuracy.

6.6 NOISE

The leads to each of the analog multiplexer input pins should be kept as short as possible. This will minimize input noise and clock frequency coupling that can cause conversion errors. Input filtering can be used to reduce the effects of the noise sources.

6.7 POWER SUPPLIES

Noise spikes on the V_A+ and V_D+ supply lines can cause conversion errors; the comparator will respond to the noise. The ADC is especially sensitive to any power supply spikes that occur during the auto-zero or linearity correction. Low inductance tantalum capacitors of 10 µF or greater paralleled with 0.1 µF monolithic ceramic capacitors are recommended for supply bypassing. Separate bypass capacitors should be used for the V_A+ and V_D+ supplies and placed as close as possible to these pins.

6.8 GROUNDING

The LM12(H)454/8's nominal performance can be maximized through proper grounding techniques. These include the use of a single ground plane and meticulously separating analog and digital areas of the board. The use of separate analog and digital digital planes within the same board area generally provides best performance. All components that handle digital signals should be placed within the digital area of the board, as defined by the digital power plane, while all analog components should be placed in the analog area of the board. Such placement and the routing of analog and digital signal lines within their own respective board areas greatly reduces the occurrence of ground loops and noise. This will also minimize EMI/RFI radiation and susceptibility.

It is recommended that stray capacitance between the analog inputs or outputs, including the reference pins, be kept to a minimum by increasing the clearance (+1/16th inch) between the analog signal and reference pins and the ground plane.

6.9 CLOCK SIGNAL CONSIDERATIONS

The LM12(H)458's performance is optimized by routing the analog input/output and reference signal conductors (pins 34–44) as far as possible from the conductor that carries the clock signal to pin 23.

Avoid overshoot and undershoot on the clock line by treating this line as a transmission line (use proper termination tech-

6.0 Design Considerations (Continued)

niques). Failure to do so can result in erratic operation. Generally, a series 30Ω to 50Ω resistor in the clock line, located as close to the clock source as possible, will prevent most problems. The clock source should drive ONLY the LM12(H)458 clock pin.

7.0 Common Application Problems

Driving the analog inputs with op-amp(s) powered from supplies other than the supply used for the LM12(H)458. This practice allows for the possibility of the amplifier output (LM12(H)458 input) to reach potentials outside of the 0V to V_A+ range. This could happen in normal operation if the amplifier use supply voltages outside of the range of the LM12(H)458 supply rails. This could also happen upon power up if the amplifier supply or supplies ramp up faster than the supply of the LM12(H)458. If any pin experiences a potential more than 100 mV below ground or above the supply voltage, even on a fast transient basis, the result could be erratic operation, missing codes, one channel interacting with one or more of the others, skipping channels or a complete malfunction, depending upon how far the input is driven beyond the supply rails.

Not performing a full calibration at power up. This can result in missing codes. The device needs to have a full calibration run *and completed* after power up and *BEFORE* attempting to perform even a single conversion or watchdog operation. The only way to recover if this is violated is to interrupt the power to the device.

Not waiting for the calibration process to complete before trying to write to the device. Once a calibration is requested, the ONLY read of the LM12(H)458 should be if the Interrupt Status Register to check for a completed calibration. Attempting a write or any other read during calibration would cause a corruption of the calibration process, resulting in missing codes. The only way to recover would be to interrupt the power.

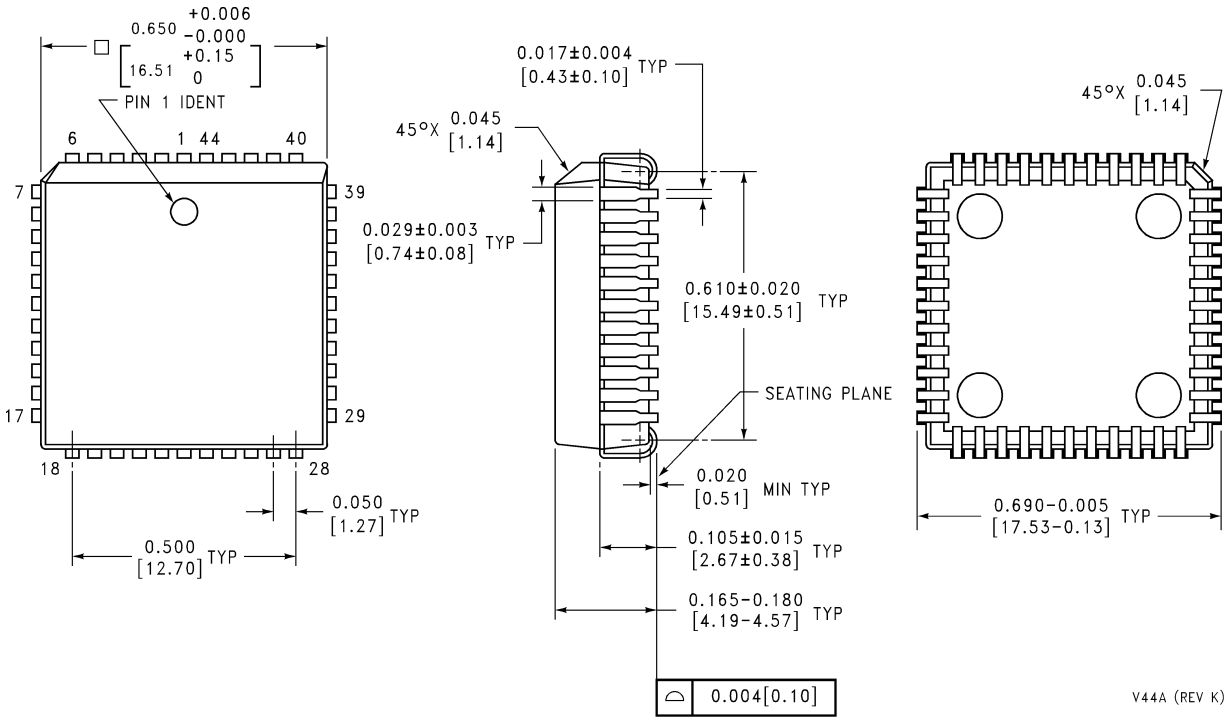
Improper termination of digital lines. Improper termination can result in energy reflections that build up to cause overshoot that goes above the supply potential and undershoot that goes below ground. It is never good to drive a device beyond the supply rails, unless the device is specifically designed to handle this situation, but the LM12(H)458 is more sensitive to this condition that most devices. Again, if any pin experiences a potential more than 100 mV below ground or above the supply voltage, even on a fast transient basis, the result could be erratic operation, missing codes, or a complete malfunction, depending upon how far the input is driven beyond the supply rails. The clock input is the most sensitive digital one. Generally, a 50Ω series resistor, located very close to the signal source, will keep digital lines "clean".

Excessive output capacitance on the digital lines. The current required to charge the capacitance on the digital outputs can cause noise on the supply bus within the LM12(H)458, causing internal supply "bounce" even when the external supply pin is pretty stable. The current required to discharge the output capacitance can cause die ground "bounce". Either of these can cause noise to be induced at the analog inputs, resulting in conversion errors.

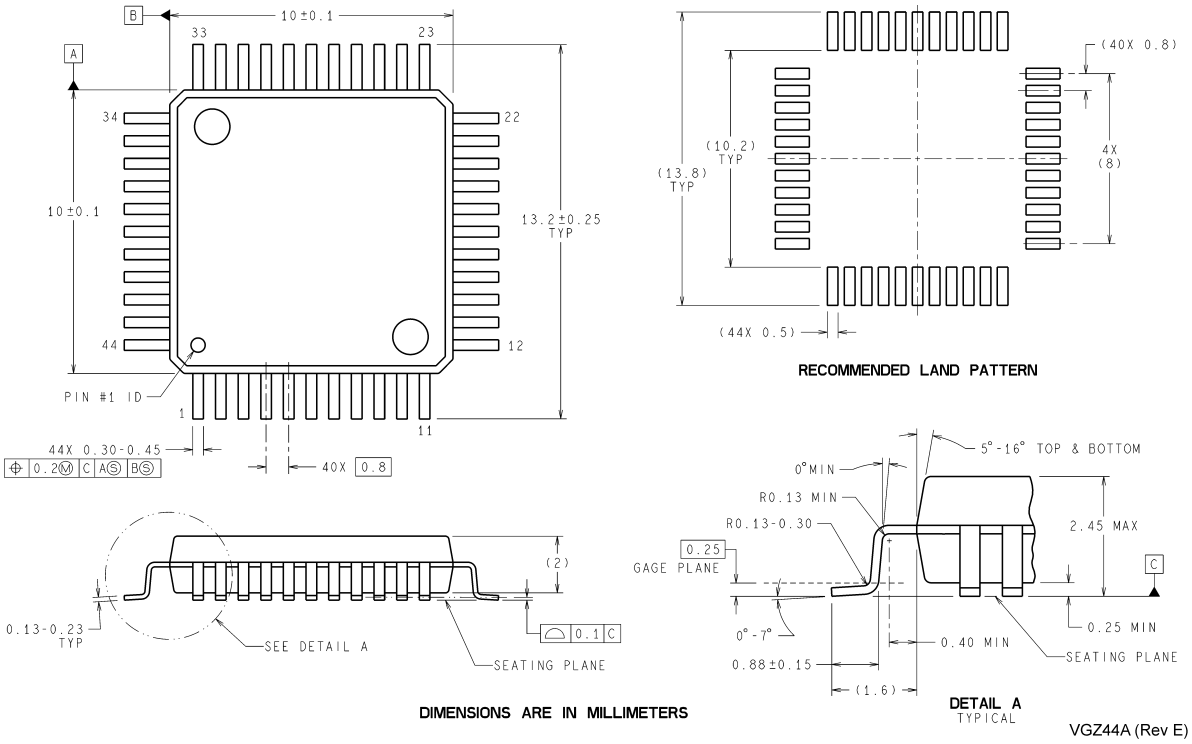
Output capacitance should be limited as much as possible. A series 100Ω resistor in each digital output line, located very close to the output pin, will limit the charge and discharge current, minimizing the extent of the conversion errors.

Improper $\overline{CS}$ decoding. If address decoder is used, care must be exercised to ensure that no "runt" (very narrow) pulse is produced on the$\overline{CS}$ line when trying to address another device or memory. Even sub-nanosecond spikes on the $\overline{CS}$ line can cause the chip to be reprogrammed in accordance with what happens to be on the data lines at the time. The result is unexpected operation. The worst case result is that the device is put into the "Test" mode and the on-board EEPROM that corrects linearity is corrupted. If this happens, the only recourse is to replace the device.

Physical Dimensions inches (millimeters) unless otherwise noted



Order Number LM12454CIV, LM12458CIV or LM12H458CIV
NS Package Number V44A



Order Number LM12H458CIVF or LM12458CIVF
NS Package Number VGZ44A

Notes

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