

# 4-channel temperature sensor IC for PCs with I<sup>2</sup>C BUS interface

## BU9817FV

The BU9817FV is a 4-channel, 8-bit, A / D converter / overvoltage detector that is perfect for temperature sensors with built-in I<sup>2</sup>C BUS interfaces. The host can access the BU9817FV anytime for the voltage data.

### ●Applications

Notebook computers, desktop computers, household electric appliances

### ●Features

- 1) By attaching a thermistor, a maximum four-channel temperature sensor is possible.
- 2) Can set comparison voltages independently.
- 3) Built-in I<sup>2</sup>C BUS interface.
- 4) Detection level and operating mode settings are programmable.
- 5) Extremely low operating current perfect for portable equipment.
- 6) Operating voltage of V<sub>DD</sub> = 3V to 5.5V.

### ●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V <sub>DD</sub>	7.0	V
Power dissipation	P <sub>d</sub>	350	mW
Operating temperature	T <sub>opr</sub>	- 15 ~ + 75	°C
Storage temperature	T <sub>stg</sub>	- 55 ~ +125	°C
Voltage applied to pins	V <sub>IN</sub>	GND - 0.5 ~ V <sub>DD</sub> + 0.5	V

\* Reduced by 3.5mW for each increase in Ta of 1°C over 25°C.

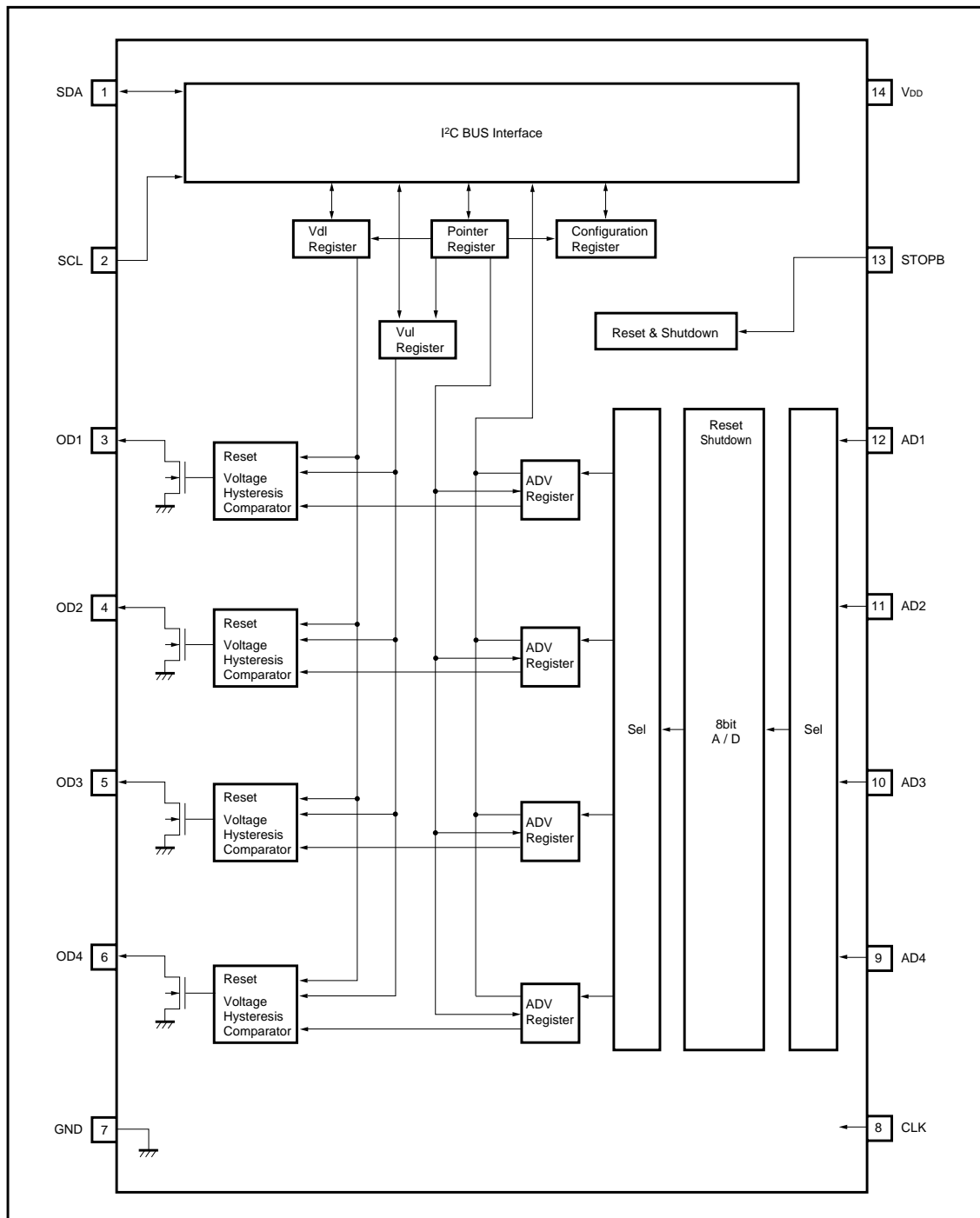
### ●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating power supply voltage	V <sub>DD</sub>	3.0	—	5.5	V

Note) I<sup>2</sup>C BUS is a registered trademark philips.

Multimedia ICs

●Block diagram



## Multimedia ICs

## ●Pin descriptions

Pin No.	Pin name	Function
1	SDA	I <sup>2</sup> C BUS Serial Data Line
2	SCL	I <sup>2</sup> C BUS Serial Clock Input
3	OD1	Open Drain Output 1
4	OD2	Open Drain Output 2
5	OD3	Open Drain Output 3
6	OD4	Open Drain Output 4
7	GND	Ground
8	CLK	Clock for Logic Input
9	AD4	Analog-to-Digital Converter Input 4
10	AD3	Analog-to-Digital Converter Input 3
11	AD2	Analog-to-Digital Converter Input 2
12	AD1	Analog-to-Digital Converter Input 1
13	STOPB	Reset & Power save mode set
14	V <sub>DD</sub>	Supply Voltage 3.0V to 5.5V

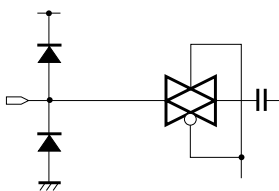
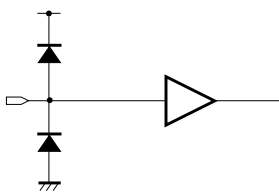
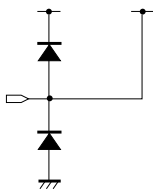
## Multimedia ICs

## ●Input / output equivalent circuits

Pin. No	Pin name	Input / output circuits	Function
1	SDA		I <sup>2</sup> C BUS serial data input / output. When only input address accords slave address (BU9817FV's), register data is inputted or outputted.
2	SCL		I <sup>2</sup> C BUS serial clock input.
3 4 5 6	OD1 OD2 OD3 OD4		Open-drain output corresponds to AD1 to AD4 input. Connect this pin a pull-up resistor. The pull-up resistor should be above $V_{DD} / 4\text{mA}$ ( $\Omega$ ).
7	GND		Ground terminal.
8	CLK		Clock input for ADC block. Input clock is 32.768kHz. AD converter and voltage hysteresis comparator use this clock to operate.

Multimedia ICs

●Input / output equivalent circuits

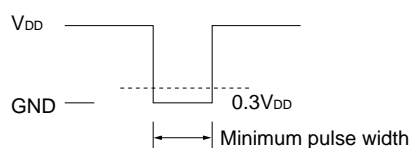
Pin. No	Pin name	Input / output circuits	Function
9 10 11 12	AD1 AD2 AD3 AD4		AD input. Each channel is converted in order. (AD1, AD2, AD3, AD4, AD1,AD2...)
13	STOPB		Reset and power save mode setting. High: Operation mode Operation follows the setting of configuration register. Low : Reset & Power save mode Reset the all internal circuit and stop the ADC operation. Go into power save mode. * Be sure to set STOPB pin low for initial reset of the internal circuit, when the BU9816FV is power up.
14	V <sub>DD</sub>		Power supply. Supply voltage 3.0V to 5.5V.

## Multimedia ICs

● Electrical characteristics (unless otherwise noted,  $V_{DD} = 5.0V$ ,  $T_a = 25^\circ C$ )

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Circuit current (normal)	$I_{CC}$	0.2	0.75	2.0	mA	SDA, SCL = "H" CLK = 32.768kHz
Circuit current (shutdown / reset / STOPB)	$I_{CC.SD}$	—	1.0	2.0	$\mu A$	SDA, SCL = "H" CLK = 32.768kHz Mode setting or STOPB = Low
Input high level voltage	$V_{IH}$	$V_{DD} \times 0.7$	$V_{DD}$	$V_{DD} + 0.5$	V	—
Input low level voltage	$V_{IL}$	-0.5	0.0	$V_{DD} \times 0.3$	V	—
Input high level current	$I_{IH}$	—	0.0	1.0	$\mu A$	—
Input low level current	$I_{IL}$	-1.0	0.0	—	$\mu A$	—
Input capacity	$C_i$	—	—	10	pF	—
Open drain output low level voltage	$V_{OLod}$	0.0	0.2	0.6	V	$I_{OL} = 4.0mA$
SDA output low level voltage	$V_{OLsda}$	0.0	0.2	0.6	V	$I_{OL} = 6.0mA$
SDA output fall time	$t_{fsda}$	—	—	250	ns	$C_L = 400pF$ $I_{OL} = 6.0mA$
STOPB minimum pulse width	$pw_{stopb}$	10	—	—	$\mu s$	—

(STOPB minimum pulse width)



(A / D)

AD resolution	RES	—	8	—	bits	—
Non-linearity error	$N_{le}$	-2	—	2	LSB	—
Differential non-linearity error	$N_{dle}$	-1	—	1	LSB	2 points connected
1-channel conversion time	$T_c$	—	305	—	$\mu s$	$f_{CLK} = 32.768kHz$
Input range	$A_i$	GND	—	$V_{DD}$	V	—

Multimedia ICs

● Measurement circuit

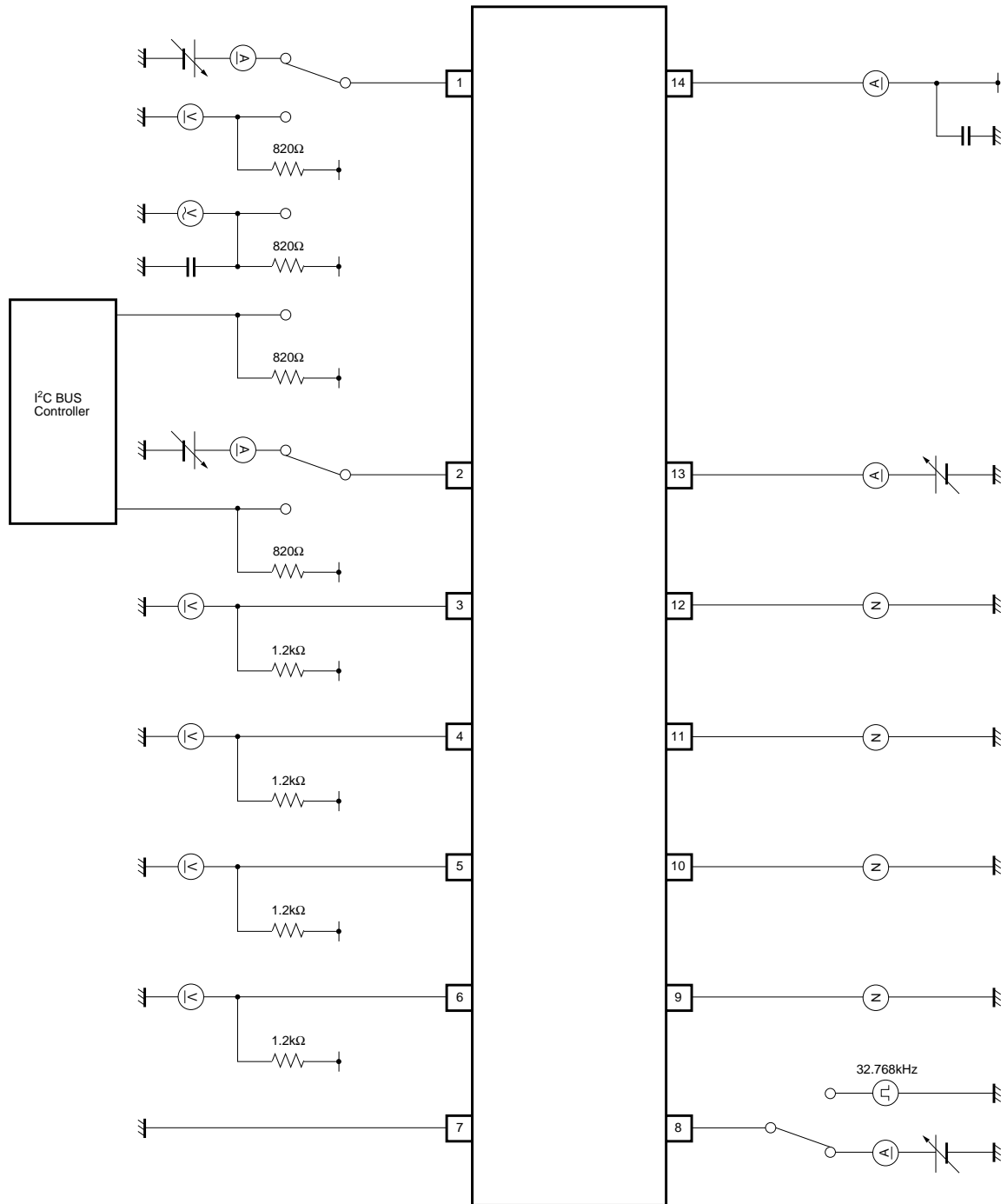


Fig.1

Multimedia ICs

●Circuit operation

Explanation of operating mode

Operating mode	Configuration register settings	ADC operation conversion interval	Open drain operation timing	Register status	Current consumption (typ.)
Normal mode	00000**0b	1.221ms	10th clock after A / D conversion	Normal operation	0.75mA
Interval High mode	00110**0b	1 second intervals	10th clock after A / D conversion	Normal operation	Note: average less than 3μA
Interval Low mode	00100**0b	4 second intervals	10th clock after A / D conversion	Normal operation	Note: average less than 2μA
Shutdown mode	00000**1b	Stopped	Hold status	Hold data	Less than 1μA
Reset mode	00**1***b	Stopped	Reset fixed at high	Data reset	Less than 1μA

The asterisk can be either 0 or 1.

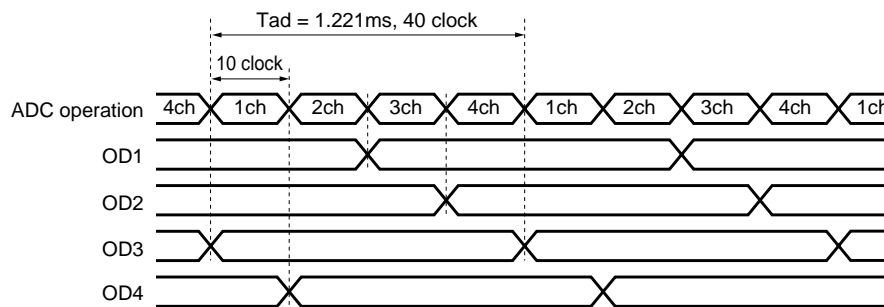
\* Conversion time is for fCLK = 32.768kHz.

\* These mode setting bits (bit 0 and bits 3 to 5) are common for each channel, the last setting of bits (bit0 and bits3 to 5) is effective for all channels. Furthermore, bits 1 and 2 are independent and can be set for each channel.

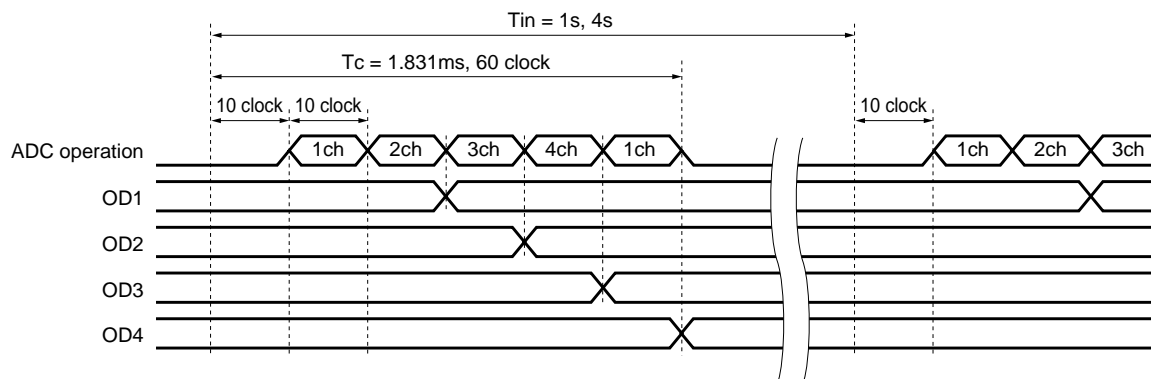
\* Note: These parameters are reference values derived through calculations and are not guaranteed characteristic values.

Explanation of ADC / open drain operation

(Normal mode)



(Interval mode)





Multimedia ICs

● Circuit operation

Explanation of I<sup>2</sup>C BUS interface

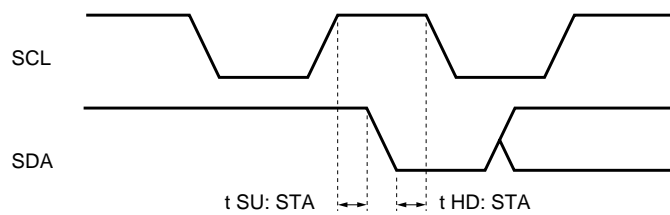
• Slave address

1	0	0	1	1	1	1	R / W
MSB							LSB

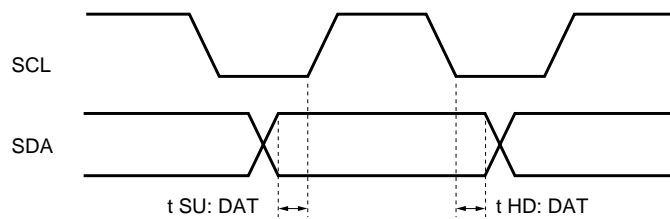
• Conforms to I<sup>2</sup>C BUS standards

Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	f SCL	0	400	kHz
Start condition hold time	t HD: STA	0.6	—	μs
Start condition setup time	t SU: STA	0.6	—	μs
Data setup time	t SU: DAT	100	—	ns
Data hold time	t HD: DAT	0	0.9	μs
Stop condition setup time	t SU: STO	0.6	—	μs

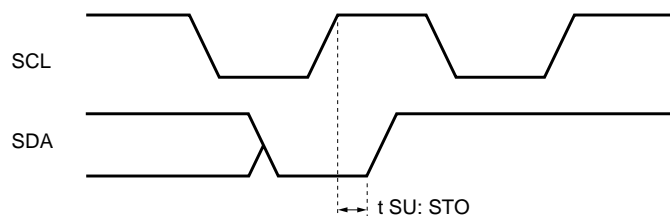
(Start conditions)



(Data conditions)



(Stop conditions)

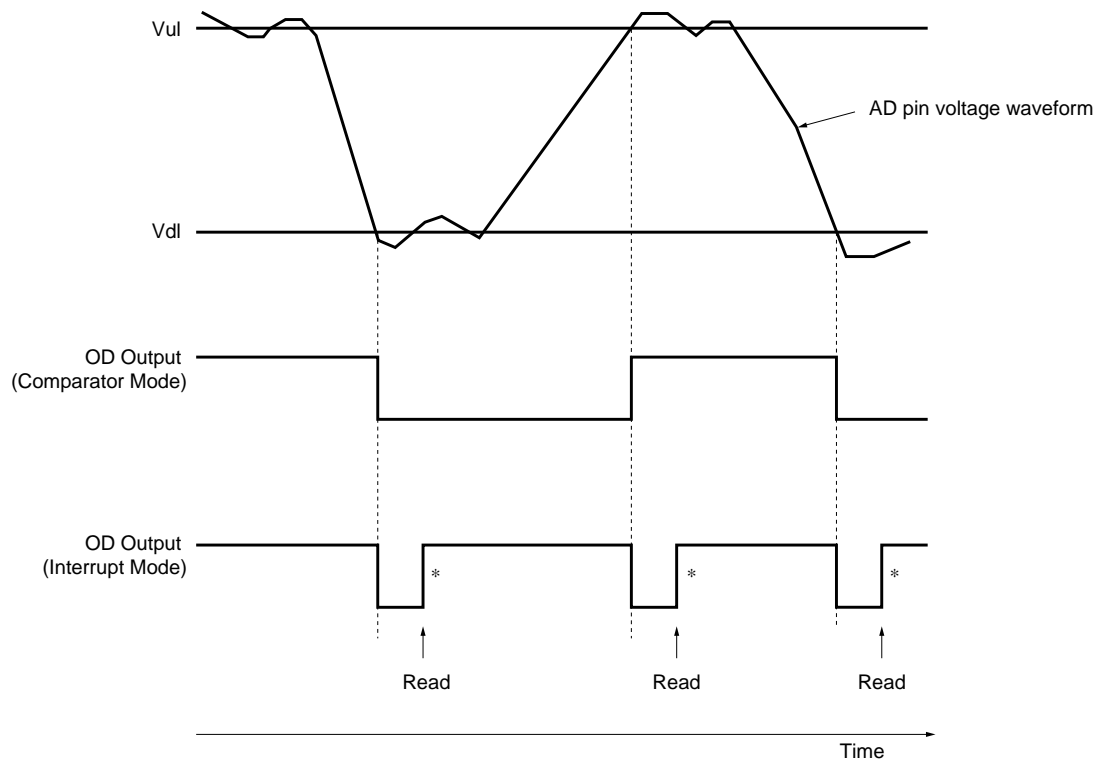


## Multimedia ICs

## ● Circuit operation

## OD output voltage response diagram

(Example: open-drain output is set active low)

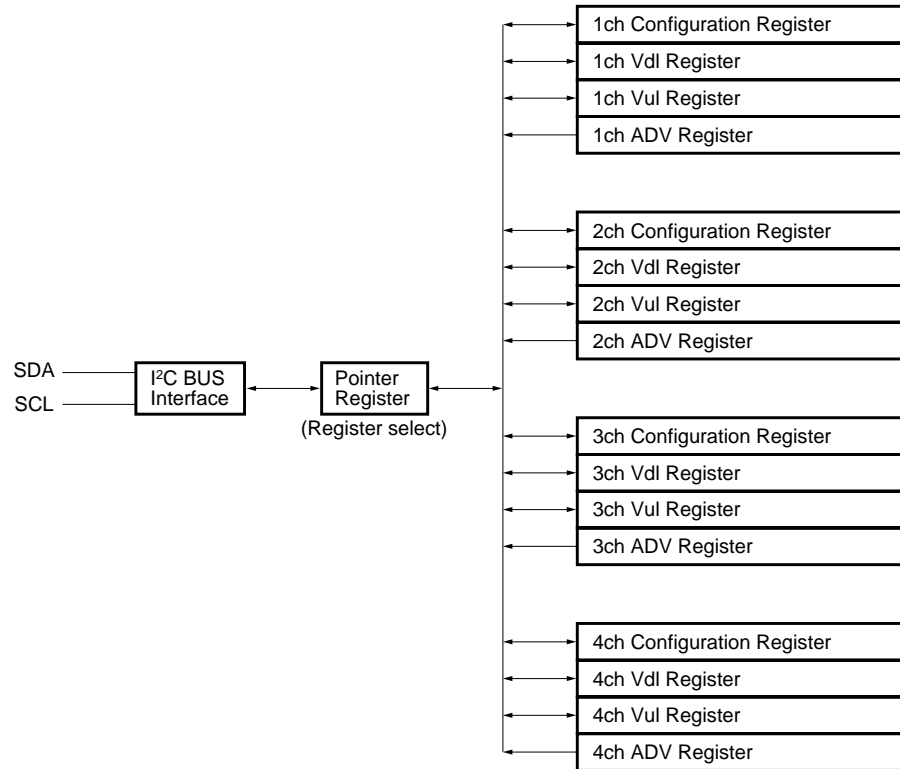


\* Note: Resetting OD output under interrupt mode occurs at only shutdown mode or reset mode or STOPB or when data read generated from host. Except for these cases, OD output is kept setting.

Multimedia ICs

●Circuit operation

Register structure



I<sup>2</sup>C Bus data structure

(1) Write Mode

S	Address	$\overline{W}$	A	Pointer reg. Byte	A	Write Data Byte	A	P
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(2) Read Mode

1) Pointer register set

S	Address	$\overline{W}$	A	Pointer reg. Byte	A
---	---------	----------------	---	-------------------	---

Sr	Address	R	A	Read Data Byte	$\overline{A}$	P
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2) Preset pointer register

S	Address	R	A	Read Data Byte	$\overline{A}$	P
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S: Start condition  
 P: Stop condition  
 Sr: Restart condition  
 A: acknowledge  
 $\overline{A}$ : acknowledge bar

## Multimedia ICs

Mode settings table 1 / 2

(1) Pointer register (selects which registers will be read from or written to)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	Channel Select		Register Select	

D4 to D7: These bits are used for test mode and must be kept zero for normal operation.

Channel Select

D3	D2	Channel
0	0	Channel 1
0	1	Channel 2
1	0	Channel 3
1	1	Channel 4

Register Select

D1	D0	Register
0	0	ADV Register (Read only) (Power on Reset default)
0	1	Configuration Register (Read / Write)
1	0	Vdl Register (Read / Write)
1	1	Vul Register (Read / Write)

(2) ADV Register (Read only)

Channel	D7	D6	D5	D4	D3	D2	D1	D0
1 ch	MSB	bit6	bit5	bit4	bit3	bit2	bit1	LSB
2 ch	MSB	bit6	bit5	bit4	bit3	bit2	bit1	LSB
3 ch	MSB	bit6	bit5	bit4	bit3	bit2	bit1	LSB
4 ch	MSB	bit6	bit5	bit4	bit3	bit2	bit1	LSB

D0 to D7: Voltage data

The defaults for the power-on-reset and reset modes are 1 for all bits.

(3) Configuration Register (Read / Write)

Channel	D7	D6	D5	D4	D3	D2	D1	D0
1 ch	0	0	Interval Mode	Interval Speed	Reset	Opendrain Polarity	Comp. / Int.	Shutdown
2 ch	0	0				Opendrain Polarity	Comp. / Int.	
3 ch	0	0				Opendrain Polarity	Comp. / Int.	
4 ch	0	0				Opendrain Polarity	Comp. / Int.	

The defaults for the power-on-reset and reset modes are 0 for all bits.

## Multimedia ICs

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### Mode settings table 2 / 2

#### D0 : Shutdown

“0” - Operation mode.

“1” - The BU9817FV stops A / D operation and goes into low power shutdown mode.

D0 bit of each channel is common bit.

#### D1 : Comparator / Interrupt mode

“0” - Comparator mode.

“1” - Interrupt mode.

#### D2 : Open Drain Polarity

“0” - active low.

“1” - active high.

#### D3 : Reset

“0” - Operation mode.

“1” - Reset any bits except D3 bit of the configuration register, any registers, the A / D converter, and the voltage hysteresis comparator.

D3 bit of each channel is common bit.

#### D4 : Interval Speed

Set the conversion cycle time of the 8bit A / D and the voltage hysteresis comparator when D5 bit (Interval Mode) is “1”.

“0” - conversion cycle time is 4s.

“1” - conversion cycle time is 1s.

D4 bit of each channel is common bit.

#### D5 : Interval Mode

“0” - normal mode.

“1” - Interval mode.

D5 bit of each channel is common bit.

### (4) Vul and Vdl Register (Read / Write)

Channel	D7	D6	D5	D4	D3	D2	D1	D0
1 ch	MSB	bit6	bit5	bit4	bit3	bit2	bit1	LSB
2 ch	MSB	bit6	bit5	bit4	bit3	bit2	bit1	LSB
3 ch	MSB	bit6	bit5	bit4	bit3	bit2	bit1	LSB
4 ch	MSB	bit6	bit5	bit4	bit3	bit2	bit1	LSB

D0 to D7: Voltage limit data of Vul and Vdl.

Default after power on reset and reset mode is Vul = 80h, Vdl = 66h.

Multimedia ICs

●Application example

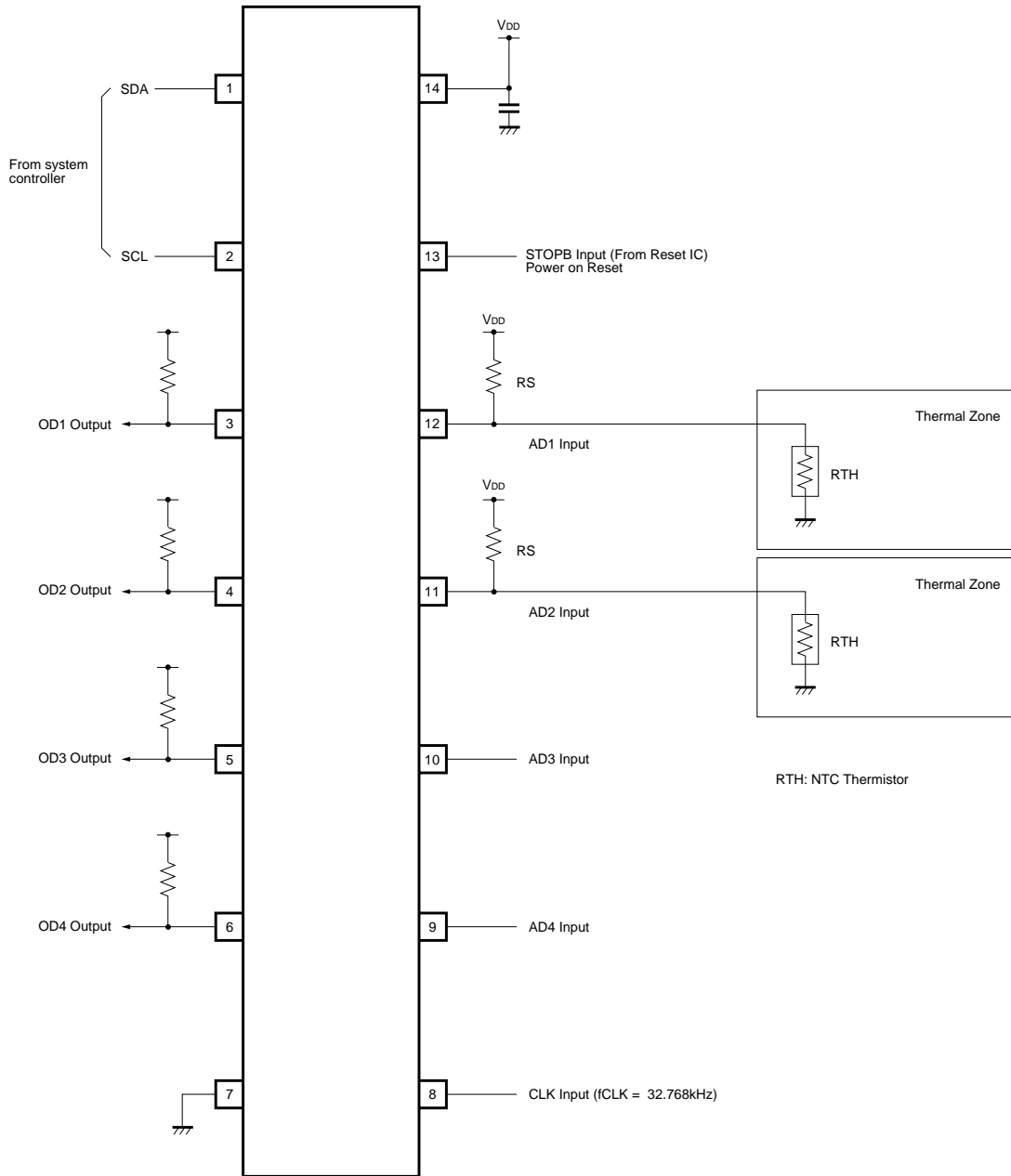


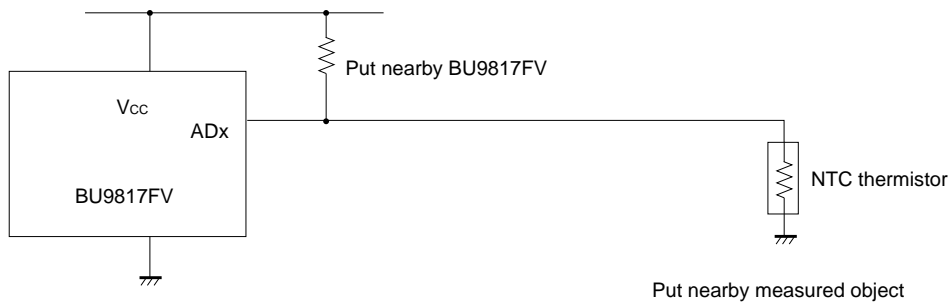
Fig.2

Multimedia ICs

●Explanation for external components

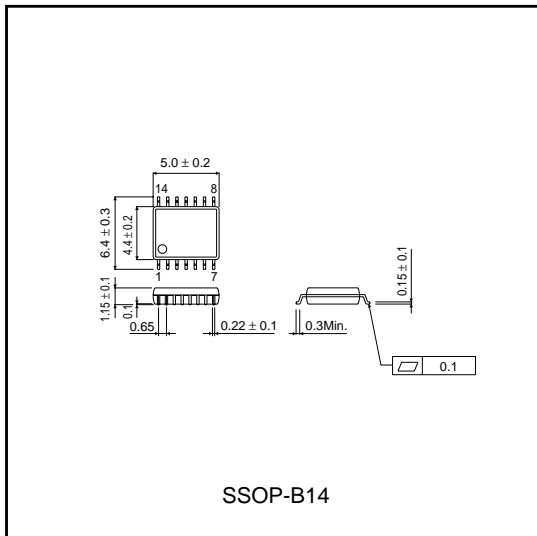
(1) AD input pin (example when used as a temperature sensor)

To the AD input pin, input a voltage with divided resistance from a resistor and NTC thermistor. For the sensor to measure the temperature, the NTC thermistor is used. The thermistor is a p-type semiconductor and as the temperature increases, the resistance value becomes lower. In other words, the resistance temperature coefficient is negative, and so the AD input pin voltage temperature characteristics are also negative.



GND is required common and stability.

●External dimensions (Units : mm)



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