NAU8401
24-bit Stereo Audio DAC with Speaker Driver

GENERAL DESCRIPTION

The NAU8401 is a low power, high quality audio output system for portable applications. In addition to precision 24-bit stereo DACs, this device integrates a broad range of additional functions to simplify implementation of complete audio systems. The NAU8401 includes drivers for speaker, headphone, and stereo line outputs, and integrates mixing of the DAC outputs with analog input signals.

Advanced on-chip digital signal processing includes a 5-band equalizer, a 3-D audio enhancer, and a digital limiter/dynamic range compressor function for the playback path. The digital interface can operate as either a master or a slave. Additionally, an internal Fractional-N PLL is available to generate accurate audio sample rate clocks for the DAC derived from any available system clock from 8MHz through 33MHz.

The NAU8401 operates with analog supply voltages from 2.5V to 3.6V, while the digital core can operate as low as 1.7V to reduce power. The loudspeaker BTL output pair and two auxiliary line outputs can use a 5V supply to increase output power capability, enabling the NAU8401 to drive 1 Watt into an external speaker. Internal control registers enable flexible power conserving modes, shutting down sub-sections of the chip under software control.

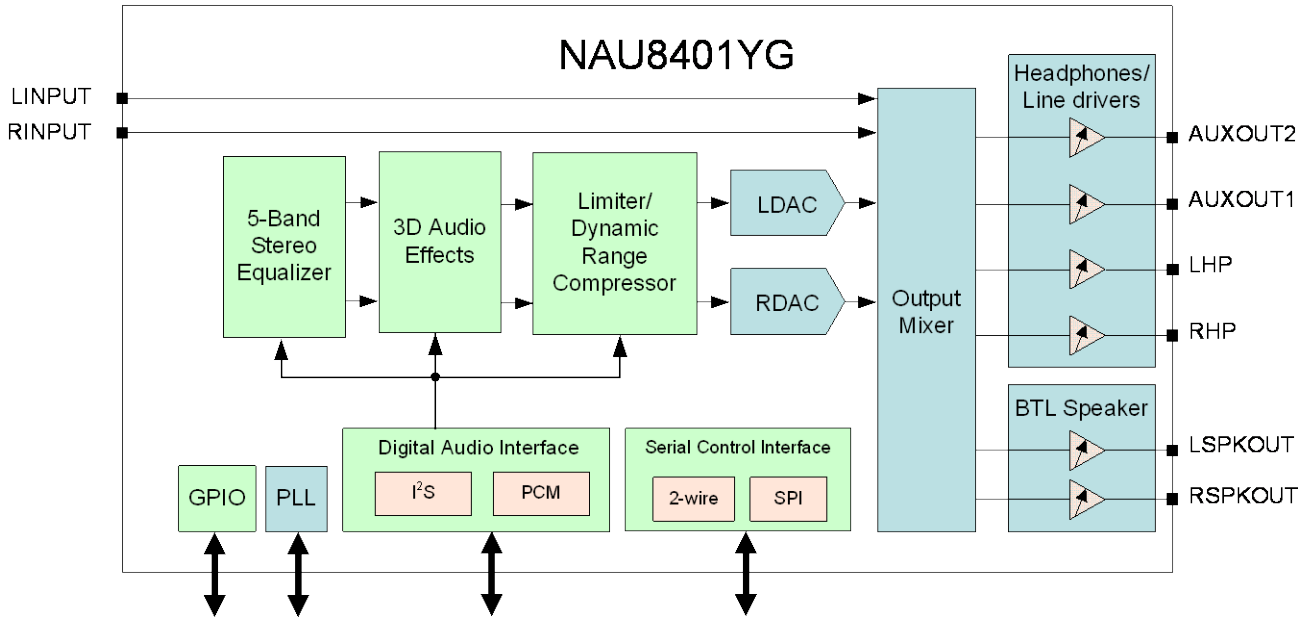
The NAU8401 is specified for operation from -40°C to +85°C. AEC-Q100 & TS16949 compliant device is available upon request.

FEATURES

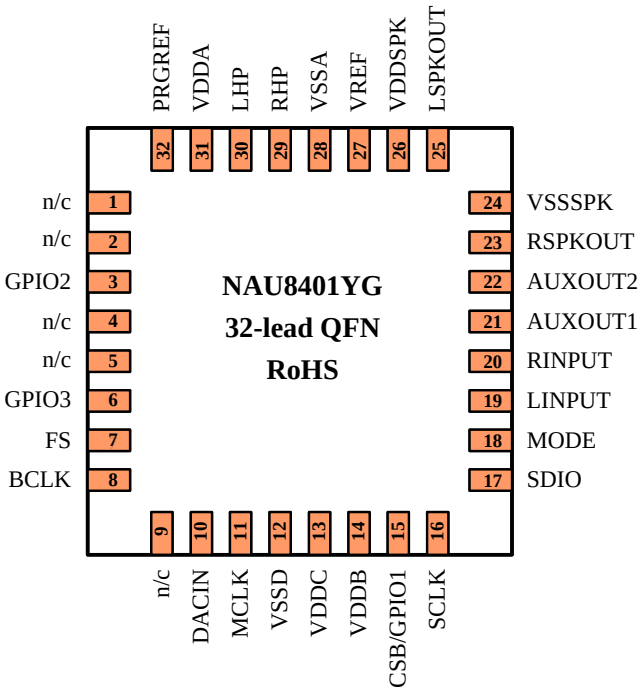
- DAC: 94dB SNR and -84dB THD ("A" weighted)
- Integrated BTL speaker driver: 1W into 8Ω
- Integrated head-phone driver: 40mW into 16Ω
- Integrated line inputs and line outputs
- On-chip high resolution Fractional-N PLL
- Integrated DSP with specific functions:
  - 5-band equalizer
  - 3-D audio enhancement
  - Automatic level control
  - Audio level limiter/dynamic range compressor
- Standard audio interfaces: PCM and I^2S
- Serial control interfaces with read/write capability
- Supports audio sample rates from 8kHz to 48kHz

Applications

- Personal Navigation Devices
- Personal Media Players
- Personal Navigation Devices
- Portable Game Players
- Portable TVs



Pinout



Part Number	Dimension	Package	Package Material
NAU8401YG	5 x 5 mm	32-QFN	Pb-Free

Pin Descriptions

Pin #	Name	Type	Functionality
1	n/c		Not internally connected
2	n/c		Not internally connected
3	GPIO2	Digital Input	General purpose I/O. Can be used for jack detect.
4	n/c		Not internally connected
5	n/c		Not internally connected
6	GPIO3	Digital Output	General Purpose I/O. Can be used for jack detect. In 4-wire mode, must be used as output to read register data.
7	FS	Digital I/O	Digital Audio DAC and ADC Frame Sync
8	BCLK	Digital I/O	Digital Audio Bit Clock
9	n/c		Not internally connected
10	DACIN	Digital Input	Digital Audio DAC Data Input
11	MCLK	Digital Input	Master Clock Input
12	VSSD	Supply	Digital Ground
13	VDDC	Supply	Digital Core Supply
14	VDDB	Supply	Digital Buffer (Input/Output) Supply
15	CSB/GPIO1	Digital I/O	3-Wire MPU Chip Select or General Purpose I/O
16	SCLK	Digital Input	3-Wire MPU Clock Input / 2-Wire MPU Clock Input
17	SDIO	Digital I/O	3-Wire MPU Data Input / 2-Wire MPU Data I/O
18	MODE	Digital Input	Control Interface Mode Selection Pin
19	LINPUT	Analog Input	Left Analog Input
20	RINPUT	Analog Input	Right Analog Input
21	AUXOUT1	Analog Output	Headphone Ground / Mono Mixed Output / Line Output
22	AUXOUT2	Analog Output	Headphone Ground / Line Output
23	RSPKOUT	Analog Output	BTL Speaker Positive Output or Right high current output
24	VSSSPK	Supply	Speaker Ground (ground pin for RSPKOUT, LSPKOUT, AUXOUT2 and AUXTOUT1 output drivers)
25	LSPKOUT	Analog Output	BTL Speaker Negative Output or Left high current output
26	VDDSPK	Supply	Speaker Supply (power supply pin for RSPKOUT, LSPKOUT, AUXOUT2 and AUXTOUT1 output drivers)
27	VREF	Reference	Decoupling for Midrail Reference Voltage
28	VSSA	Supply	Analog Ground
29	RHP	Analog Output	Headphone Positive Output / Line Output Right
30	LHP	Analog Output	Headphone Negative Output / Line Output Left
31	VDDA	Supply	Analog Power Supply
32	PRGREF	Analog Output	Programmable buffered DC voltage output
33	GPAD	Bulk Ground Pad	Electrical and Thermal pad on underside of device

Notes

1. The 32-QFN package includes a bulk ground connection pad on the underside of the device. This bulk ground should be thermally tied to the PCB as much as possible, and electrically tied to the analog ground (VSSA, pin 28).
2. Unused analog input pins should be left as no-connection.
3. Unused digital input pins should be tied to ground.
4. Pins designated as "n/c" (Not Internally Connected) should be left as no-connection

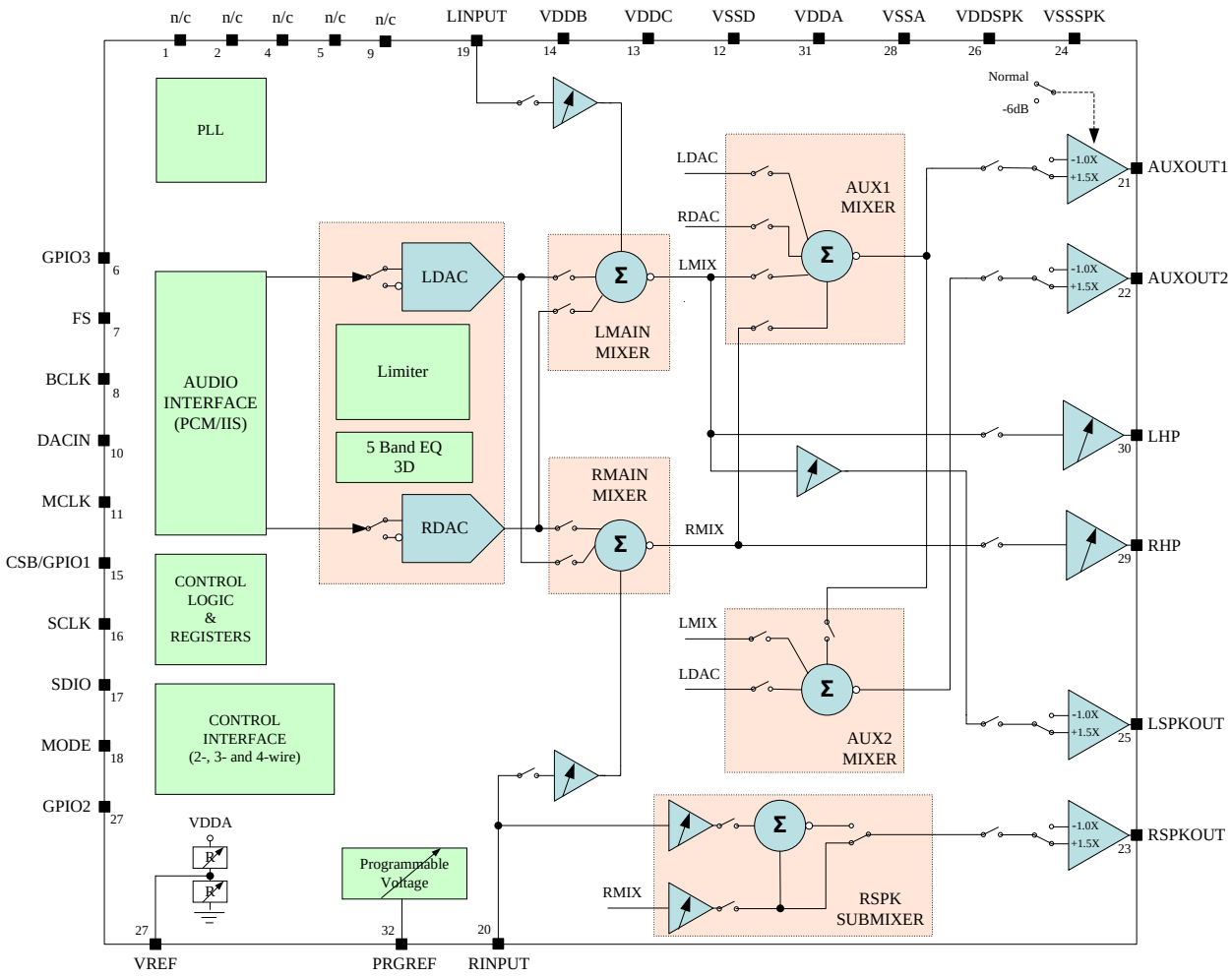


Figure 1: NAU8401 Block Diagram

Table of Contents

Electrical Characteristics

Conditions: VDDC = 1.8V, VDDA = VDDB = VDDSPK = 3.3V, MCLK = 12.288MHz,
T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data, unless otherwise stated.

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Digital to Analog Converter (DAC) driving RHP / LHP with 10kΩ / 50pF load						
Full scale output [1]				VDDA / 3.3		V_{rms}
Signal-to-noise ratio	SNR	A-weighted	88	94		dB
Total harmonic distortion [2]	THD+N	R_L = 10kΩ; full-scale signal		-84		dB
Channel separation		1kHz signal		99		dB
Power supply rejection ratio (50Hz - 22kHz)	PSRR			53		dB
Speaker Output (RSPKOUT / LSPKOUT with 8Ω bridge-tied-load)						
Full scale output [3]		SPKBST = 1 VDDSPK = VDDA		VDDA / 3.3		V_{rms}
		SPKBST = 0 VDDSPK = VDDA * 1.5		(VDDA / 3.3) * 1.5		V_{rms}
Total harmonic distortion [2]	THD+N	P_o = 320mW, VDDSPK=3.3V		-64		dB
		P_o = 400mW, VDDSPK = 3.3V		-60		dB
		P_o = 860mW, VDDSPK = 5.0V		-60		dB
		P_o = 1000mW, VDDSPK = 5.0V		-34		dB
Signal-to-noise ratio	SNR	VDDSPK = 3.3V		91		dB
Power supply rejection ratio (50Hz - 22kHz)	PSRR			81		dB
Maximum programmable gain				+6		dB
Minimum programmable gain				-57		dB
Programmable gain step size		Guaranteed monotonic		1		dB
Mute attenuation		1kHz full scale signal		85		dB
Headphone Output (RHP / LHP with 32Ω load)						
0dB full scale output voltage				VDDA / 3.3		V_{rms}
Signal-to-noise ratio	SNR	A-weighted		92		dB
Total harmonic distortion [2]	THD+N	R_L = 16Ω, P_o = 20mW, VDDA = 3.3V		80		dB
		R_L = 32Ω, P_o = 20mW, VDDA = 3.3V		85		dB
Maximum programmable gain				+6		dB
Minimum programmable gain				-57		dB
Programmable gain step size		Guaranteed monotonic		1		dB
Mute attenuation		1kHz full scale signal		85		dB
AUXOUT1 / AUXOUT2 with 10kΩ / 50pF load						
Full scale output [3]		AUX1BST = 1 AUX2BST = 1 VDDSPK = VDDA		VDDA / 3.3		V_{rms}
		AUX1BST = 0 AUX2BST = 0 VDDSPK = VDDA * 1.5		(VDDA / 3.3) * 1.5		V_{rms}
Signal-to-noise ratio	SNR			87		dB
Total harmonic distortion [2]	THD+N			-83		dB
Channel separation		1kHz signal		99		dB
Power supply rejection ratio (50Hz - 22kHz)	PSRR			53		dB

Electrical Characteristics, cont'd.

Conditions: VDDC = 1.8V, VDDA = VDDB = VDDSPK = 3.3V, MCLK = 12.288MHz,
T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data, unless otherwise stated.

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Line Level Analog Inputs (LINPUT, RINPUT)						
Full scale input signal [1]		Gain = 0dB		1.0 0		Vrms dBV
Input resistance		Aux direct-to-out path, only Input gain = +6.0dB Input gain = 0.0dB Input gain = -12dB		 20 40 159		 kΩ kΩ kΩ
Input capacitance				10		pF
PRGREF programmable reference voltage						
Output voltage	V_{PRGREF}	See Figure 3	0.50, 0.60,0.65, 0.70, 0.75, 0.85, or 0.90			VDDA VDDA
Output current	I_{PRGREF}			3		mA
Output noise voltage	V_n	1kHz to 20kHz		14		nV/√Hz
Digital Input/Output						
Input HIGH level	V_{IL}		0.7 * VDDB			V
Input LOW level	V_{IH}				0.3 * VDDB	V
Output HIGH level	V_{OH}	I_{Load} = 1mA	0.9 * VDDB			V
Output LOW level	V_{OL}	I_{Load} = -1mA			0.1 * VDDB	V
Input capacitance				10		pF

Notes

1. Full Scale is relative to the magnitude of VDDA and can be calculated as FS = VDDA/3.3.
2. Distortion is measured in the standard way as the combined quantity of distortion products plus noise. The signal level for distortion measurements is at 3dB below full scale, unless otherwise noted.
3. With default register settings, VDDSPK should be 1.5xVDDA (but not exceeding maximum recommended operating voltage) to optimize available dynamic range in the AUXOUT1 and AUXOUT2 line output stages. Output DC bias level is optimized for VDDSPK = 5.0Vdc (boost mode) and VDDA = 3.3Vdc.

Absolute Maximum Ratings

Condition	Min	Max	Units
VDDB, VDDC, VDDA supply voltages	-0.3	+3.61	V
VDDSPK supply voltage (default register configuration)	-0.3	+5.80	V
VDDSPK supply voltage (optional low voltage configuration)	-0.3	+3.61	V
Core Digital Input Voltage range	VSSD – 0.3	VDDC + 0.30	V
Buffer Digital Input Voltage range	VSSD – 0.3	VDDB + 0.30	V
Analog Input Voltage range	VSSA – 0.3	VDDA + 0.30	V
Industrial operating temperature	-40	+85	°C
Storage temperature range	-65	+150	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely influence product reliability and result in failures not covered by warranty.

Operating Conditions

Condition	Symbol	Min	Typical	Max	Units
Digital supply range (Core)	VDDC	1.65		3.60	V
Digital supply range (Buffer)	VDDB	1.65		3.60	V
Analog supply range	VDDA	2.50		3.60	V
Speaker supply required: SPKBST=AUX1BST=AUX2BST = 0	VDDSPK	2.50		5.50	V
Speaker supply if any: SPKBST, AUX1BST, or AUX2BST = 1	VDDSPK	2.50		3.60	V
Ground	VSSD VSSA VSSSPK		0		V

1. VDDA must be ≥ VDDC.
2. VDDB must be ≥ VDDC.

1 General Description

The NAU8401 is a stereo device with identical left and right channels that share common support elements. Additionally, the right channel auxiliary output path includes a dedicated submixer that supports mixing the right auxiliary input directly into the right speaker output driver. This enables the right speaker channel to output audio that is not present on any other output.

1.1.1 Analog Inputs

The left and right analog inputs have available analog input gain conditioning of -15dB through +6dB in 3dB steps. These inputs include individual muting functions with excellent channel isolation and off-isolation, and are suitable for full quality, high bandwidth signals.

1.1.2 Analog Outputs

There are six high current analog audio outputs. These are very flexible outputs that can be used individually or in stereo pairs for a wide range of end uses. However, these outputs are optimized for specific functions and are described in this section using the functional names that are applicable to those optimized functions.

Each output receives its signal source from built-in analog output mixers. These mixers enable a wide range of signal combinations, including muting of all sources. Additionally, each output has a programmable gain function, output mute function, and output disable function.

The RHP and LHP headphone outputs are optimized for driving a stereo pair of headphones, and are powered from the main analog voltage supply rail, VDDA. These outputs may be coupled using traditional DC blocking series capacitors. Alternatively, these may be configured in a no-capacitor DC coupled design using a virtual ground at ½ VDDA provided by an AUXOUT analog output operating in the non-boost output mode.

The AUXOUT1 and AUXOUT2 analog outputs are powered from the VDDSPK supply rail and VSSSPK ground return path. The supply rail may be the same as VDDA, or may be a separate voltage up to 5.5Vdc. This higher voltage enables these outputs to have an increased output voltage range and greater output power capability.

The RSPKOUT and LSPKOUT loudspeaker outputs are powered from the VDDSPK power supply rail and VSSGND ground return path. LSPKOUT receives its audio signal via an additional submixer. This submixer supports combining a traditional alert sound (from the RINPUT input) with the right channel headphone output mixer signal. This submixer also provides the signal invert function that is necessary for the normal BTL (Bridge Tied Load) configuration used to drive a high power external loudspeaker. Alternatively, each loudspeaker output may be used individually as a separate high current analog output driver.

1.1.3 DAC and Digital Signal Processing

Each left and right channel has an independent high quality DAC associated with it. These are high performance, 24-bit delta-sigma converters that are suitable for a very wide range of applications.

The DAC functions are each individually supported by powerful analog mixing and routing. The DAC blocks are also supported by advanced digital signal processing subsystems that enable a very wide range of programmable signal conditioning and signal optimizing functions. All digital processing is with 24-bit precision, as to minimize processing artifacts and maximize the audio dynamic range supported by the NAU8401.

The DACs are supported by a programmable limiter/DRC (Dynamic Range Compressor). This is useful to optimize the output level for various applications and for use with small loudspeakers. This is an optional feature that may be programmed to limit the maximum output level and/or boost an output level that is too small.

Digital signal processing is also provided for a 3D Audio Enhancement function, and for a 5-Band Equalizer. These features are optional, and are programmable over wide ranges. This pair of digital processing features may be applied jointly to the DAC audio path, or be jointly disabled from the DAC audio path.

1.1.4 Programmable Voltage Reference

The filtered Vref pin is buffered and scaled to create a low-noise programmable DC output voltage. This output may be used for a wide range of purposes, such as providing a DC bias for other amplifiers and components in the system.

1.1.5 Digital Interfaces

Command and control of the device is accomplished using a 2-wire/3-wire/4-wire serial control interface. This is a simple, but highly flexible interface that is compatible with many commonly used command and control serial data protocols and host drivers.

Digital audio input/output data streams are transferred to and from the device separately from command and control. The digital audio data interface supports either I2S or PCM audio data protocols, and is compatible with commonly used industry standard devices that follow either of these two serial data formats.

1.1.6 Clock Requirements

The clocking signals required for the audio signal processing, audio data I/O, and control logic may be provided externally, or by optional operation of a built-in PLL (Phase Locked Loop). An external master clock (MCLK) signal must be active for analog audio logic paths to align with control register updates, and is required as the reference clock input for the PLL, if the PLL is used.

The PLL is provided as a low cost, zero external component count optional method to generate required clocks in almost any system. The PLL is a fractional-N divider type design, which enables generating accurate desired audio sample rates derived from a very wide range of commonly available system clocks.

The frequency of the system clock provided as the PLL reference frequency may be any stable frequency in the range between 8MHz and 33MHz. Because the fractional-N multiplication factor is a very high precision 24-bit value, any desired sample rate supported by the NAU8401 can be generated with very high accuracy, typically limited by the accuracy of the external reference frequency. Reference clocks and sample rates outside of these ranges are also possible, but may involve performance tradeoffs and increased design verification.

2 Power Supply

This device has been designed to operate reliably using a wide range of power supply conditions and power-on/power-off sequences. There are no special requirements for the sequence or rate at which the various power supply pins change. Any supply can rise or fall at any time without harm to the device. However, pops and clicks may result from some sequences. Optimum handling of hardware and software power-on and power-off sequencing is described in more detail in the Applications section of this document.

2.1.1 Power-On Reset

The NAU8401 does not have an external reset pin. The device reset function is automatically generated internally when power supplies are too low for reliable operation. The internal reset is generated any time that either VDDA or VDDC is lower than is required for reliable maintenance of internal logic conditions. The reset threshold voltage for VDDA and VDDC is approximately 0.5Vdc. If both VDDA and VDDC are being reduced at the same time, the threshold voltage may be slightly lower. Note that these are much lower voltages than are required for normal operation of the chip. These values are mentioned here as general guidance as to overall system design.

If either VDDA or VDDC is below its respective threshold voltage, an internal reset condition is asserted. During this time, all registers and controls are set to the hardware determined initial conditions. Software access during this time will be ignored, and any expected actions from software activity will be invalid.

When both VDDA and VDDC reach a value above their respective thresholds, an internal reset pulse is generated which extends the reset condition for an additional time. The duration of this extended reset time is approximately 50 microseconds, but not longer than 100 microseconds. The reset condition remains asserted during this time. If either VDDA or VDDC at any time becomes lower than its respective threshold voltage, a new reset condition will result. The reset condition will continue until both VDDA and VDDC again higher than their respective thresholds. After VDDA and VDDC are again both greater than their respective threshold voltage, a new reset pulse will be generated, which again will extend the reset condition for not longer than an additional 100 microseconds.

2.1.2 Power Related Software Considerations

There is no direct way for software to determine that the device is actively held in a reset condition. If there is a possibility that software could be accessing the device sooner than 100 microseconds after the VDDA and VDDC supplies are valid, the reset condition can be determined indirectly. This is accomplished by writing a value to any register other than register 0x00, with that value being different than the power-on reset initial values. The optimum choice of register for this purpose may be dependent on the system design, and it is recommended the system engineer choose the register and register test bit for this purpose. After writing the value, software will then read back the same register. When the register test bit reads back as the new value, instead of the power-on reset initial value, software can reliably determine that the reset condition has ended.

Although it is not required, it is strongly recommended that a Software Reset command should be issued after power-on and after the power-on reset condition is ended. This will help insure reliable operation under every power sequencing condition that could occur.

If there is any possibility that VDDA or VDDC could be unreliable during system operation, software may be designed to monitor whether a power-on reset condition has happened. This can be accomplished by writing a test bit to a register that is different from the power-on initial conditions. This test bit should be a bit that is never used for any other reason, and does not affect desired operation in any way. Then, software at any time can read this bit to determine if a power-on reset condition has occurred. If this bit ever reads back other than the test value, then software can reliably know that a power-on reset event has occurred. Software can subsequently re-initialize the device and the system as required by the system design.

2.1.3 Software Reset

All chip registers can be reset to power-on default conditions by writing any value to register 0, using any of the control modes. Writing valid data to any other register disables the reset, but all registers need to have the correct operating data written. See the applications section on powering NAU8401 up for information on avoiding pops and clicks after a software reset.

3 Input Path Detailed Description

The NAU8401 provides two analog inputs that are buffered, scaled, optionally muted, and then made available to the output mixers. The output mixers enable a wide range of possible routing of these inputs to the analog output pins, as well as mixing with the output signal from the DAC subsystem.

These inputs are maintained at a DC bias at approximately ½ of the AVDD supply voltage. Connections to these inputs should be AC-coupled by means of DC blocking capacitors suitable for the device application. If not used, these input pins should not be left not-connected and muted in the software register controls.

The RINPUT signal may additionally be routed to the Right Speaker Submixer in the analog output section. This path enables a sound to be output from the LSPKOUT speaker output, but without being audible anywhere else in the system. One purpose of this path is to support a traditional "beep" sound, such as from a microprocessor toggle bit. This is a historical application scenario which is now uncommon.

These inputs are affected by the following registers:

LMAIN MIXER or RMAIN MIXER if used (see output mixer section)
RSPK SUBMIXER if used (see Right Speaker Submixer section)

3.1 Analog Input Impedance and Variable Gain Stage Topology

Each analog input pin is supported by the circuit shown here as a simplified schematic. The gain value changes affect input impedance as detailed in this section. If a path is in the "not selected" condition, then the input impedance will be in a high impedance condition and the input signal will be muted. If an external input pin is not used anywhere in the system, it will be coupled to a DC tie-off of approximately 30kΩ coupled to VREF. The unused input tie-off function is explained in more detail in the Application Information section of this document.

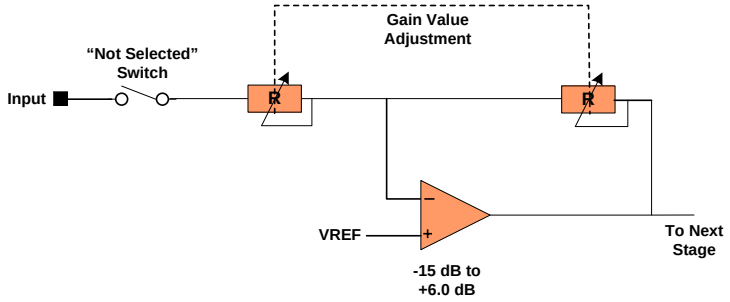


Figure 2: Variable Gain Stage Simplified Schematic

The input impedance presented to these inputs depends on the input routing choices and gain values. The nominal resistive input impedances presented to signal pins that are directly routed to an output mixer are listed in the following table. The RINPUT signal may also be connected to the Right Speaker Submixer. If both RINPUT signal paths are connected, then the RINPUT input impedance will be the parallel combination of the two paths.

Inputs	Gain (dB)	Impedance (kΩ)
LINPUT & RINPUT to bypass amp Or RINPUT to RSPK SUBMIXER amp	-15	225
	-12	159
	-9	113
	-6	80
	-3	57
	0	40
	3	28
	6	20

Table 1: Analog Input and RSPK SUBMIXER Input Impedances

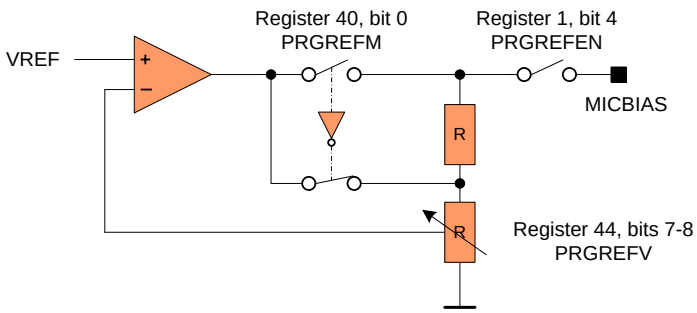
3.2 Programmable Reference Voltage Controls

The PRGREF pin provides a low-noise DC bias voltage as may be required for other elements in the audio subsystem. This built-in feature can typically provide up to 3mA of bias current. This DC bias voltage is also suitable for powering either traditional ECM (electret) type microphones, or for MEMS types microphones with an independent power supply pin.

Seven different bias voltages are available for optimum system performance, depending on the specific application. The bias pin normally requires an external filtering capacitor as shown on the schematic in the Application section. The programmable voltage bias function is controlled by the following registers:

R1 Power control for PRGREF feature (enabled when bit 4 = 1)
R44 Optional low-noise mode and different bias voltage levels (enabled when bit 0 = 1)
R44 Primary PRGREF voltage selection

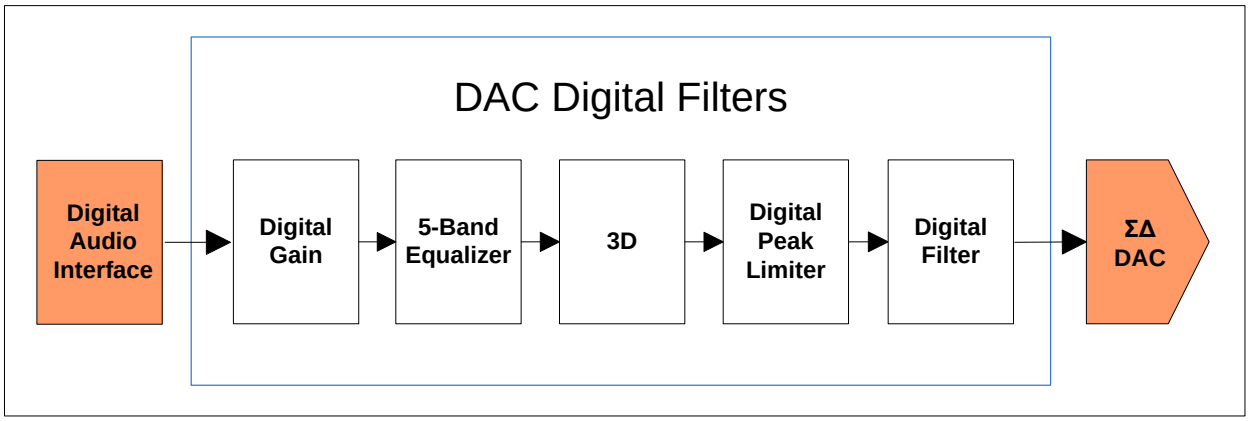
The low-noise feature results in greatly reduced noise in the external PRGREF voltage by placing a resistor of approximately 200-ohms in series with the output pin. This creates a low pass filter in conjunction with the external reference voltage filter capacitor, but without any additional external components. The low noise feature is enabled when the mode control bit 0 in register R40 is set (level = 1)



Register 44, Bits 7-8	Register 44, Bit 0	Output DC Bias Voltage
00	0	0.90 * VDDA
01	0	0.65 * VDDA
10	0	0.75 * VDDA
11	0	0.50 * VDDA
00	1	0.85 * VDDA
01	1	0.60 * VDDA
10	1	0.70 * VDDA
11	1	0.50 * VDDA

Figure 3: Programmable Reference Bias Generator

4 DAC Digital Block



The DAC digital block uses 24-bit signal processing to generate analog audio with a 16-bit digital sample stream input. This block consists of a sigma-delta modulator, digital decimator/filter, and optional 5-band graphic equalizer/3D effects block, and a dynamic range compressor/limiter. The DAC coding scheme is in twos complement format and the full-scale output level is proportional to VDDA. With a 3.3V supply voltage, the full-scale output level is $1.0V_{RMS}$.

Registers that affect the DAC operation are:

R3 Power management enable/disable left/right DAC
R7 Sample rate indication bits (affect filter frequency scaling)
R10 Softmute, Automute, oversampling options, polarity controls for left/right DAC
R11 Left channel DAC digital volume value; update bit feature
R12 Right channel DAC digital volume value; update bit feature

4.1 DAC Soft Mute

Both DACs are initialized with the SoftMute function disabled, which is a shared single control bit. Softmute automatically ramps the DAC digital volume down to zero volume when enabled, and automatically ramps the DAC digital volume up to the register specified volume level for each DAC when disabled. This feature provides a tool that is useful for using the DACs without introducing pop and click sounds.

4.2 DAC AutoMute

The analog output of both DACs can be automatically muted in a no signal condition. Both DACs share a single control bit for this function. When automute is enabled, the analog output of the DAC will be muted any time there are 1024 consecutive audio sample values with a zero value. If at any time there is a non-zero sample value, the DAC will be un-muted, and the 1024 count will be reinitialized to zero.

4.3 DAC Sampling / Oversampling Rate, Polarity Control, Digital Passthrough

The sampling rate of the DAC is determined entirely by the frequency of its input clock and the oversampling rate setting. The oversampling rate of the DAC can be changed to 128X for improved audio performance at slightly higher power consumption. Because the additional supply current is only 1mA, in most applications the 128X oversampling is preferred for maximum audio performance.

The polarity of either DAC output signal can be changed independently on either DAC analog output as a feature sometimes useful in management of the audio phase. This feature can help minimize any audio processing that may be otherwise required as the data are passed to other stages in the system.

4.4 DAC Digital Volume Control and Update Bit Functionality

The effective output audio volume of each DAC can be changed using the digital volume control feature. This processes the output of the DAC to scale the output by the amount indicated in the volume register setting. Included is a "digital mute" value which will completely mute the signal output of the DAC. The digital volume setting can range from 0dB through -127dB in 0.5dB steps.

Important: The R11 and R12 update bits are write-only bits. The primary intended purpose of the update bit is to enable simultaneous changes to both the left and right DAC volume values, even though these values must be written sequentially. When there is a write operation to either R11 or R12 volume settings, but the update bit is not set (value = 0), the new volume setting is stored as pending for the future, but does not go into effect. When there is a write operation to either R11 or R12 and the update bit is set (value = 1), then the new value in the register being written is immediately put into effect, and any pending value in the other DAC volume register is put into effect at the same time.

4.5 DAC Automatic Output Peak Limiter / Volume Boost

Both DACs are supported by a digital output volume limiter/boost feature which can be useful to keep output levels within a desired range without any host/processor intervention. Settings are shared by both DAC channels.

Registers that manage the peak limiter and volume boost functionality are:

R24 Limiter enable/disable, limiter attack rate, boost decay rate
R25 Limiter upper limit, limiter boost value

The operation of the peak limiter is shown in the following figure. The upper signal graphs show the time varying level of the input and output signals, and the lower graph shows the gain characteristic of the limiter. When the signal level exceeds the limiter threshold value by 0.5dB or greater, the DAC digital signal level will be attenuated at a rate set by the limiter attack rate value. When the input signal level is less than the boost lower limit by 0.5dB or greater, the DAC digital volume will be increased at a rate set by the boost decay rate value. The default boost gain value is limited not to exceed 0dB (zero attenuation).

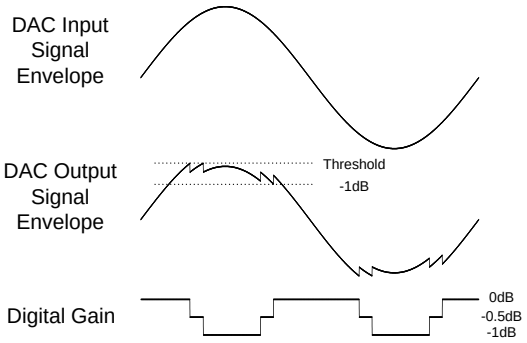


Figure 4: DAC Digital Limiter Control

The limiter may optionally be set to automatically boost the DAC digital signal level when the signal is more than 0.5dB below the limiter threshold. This can be useful in applications in which it is desirable to compress the signal dynamic range. This is accomplished by setting the limiter boost register bits to a value greater than zero. If the limiter is disabled, this boost value will be applied to the DAC digital output signal separate from other gain affecting values.

4.6 5-Band Equalizer

The NAU8401 includes a 5-band graphic equalizer with low distortion, low noise, and wide dynamic range. The equalizer is applied to both left and right channels. The equalizer is grouped with the 3D Stereo Enhancement signal processing function. These functions are applied to the DAC output signals, only, and do not affect the LINPUT and RINPUT analog input signals.

Registers that affect operation of the 5-Band Equalizer are:

R18 Enable / Disable Equalizer function
R18 Band 1 gain control and cut-off frequency
R19 Band 2 gain control, center cut-off frequency, and bandwidth
R20 Band 3 gain control, center cut-off frequency, and bandwidth
R21 Band 4 gain control, center cut-off frequency, and bandwidth
R22 Band 5 gain control and cut-off frequency

Each of the five equalizer bands is independently adjustable for maximum system flexibility, and each offers up to 12dB of boost and 12dB of cut with 1dB resolution. The high and the low bands are shelving filters (high-pass and low-pass, respectively), and the middle three bands are peaking filters. Details of the register value settings are described below. Response curve examples are provided in the Appendix of this document.

Register Value	Equalizer Band				
	1 (High Pass) Register 18 Bits 5 & 6 EQ1CF	2 (Band Pass) Register 19 Bits 5 & 6 EQ2CF	3 (Band Pass) Register 20 Bits 5 & 6 EQ3CF	4 (Band Pass) Register 21 Bits 5 & 6 EQ4CF	5 (Low Pass) Register 22 Bits 5 & 6 EQ5CF
00	80Hz	230Hz	650Hz	1.8kHz	5.3kHz
01	105Hz	300Hz	850Hz	2.4kHz	6.9kHz
10	135Hz	385Hz	1.1kHz	3.2kHz	9.0kHz
11	175Hz	500Hz	1.4kHz	4.1kHz	11.7kHz

Table 2: Equalizer Center/Cutoff Frequencies

Register Value		Gain	Registers
Binary	Hex		
00000	00h	+12db	Bits 0 to 4 in registers 18 (EQ1GC) 19 (EQ2GC) 20 (EQ3GC) 21 (EQ4GC) 22 (EQ5GC)
00001	01h	+11dB	
00010	02h	+10dB	
- - -	- -	Increments 1dB per step	
01100	0Ch	0dB	
01101	17h	-11dB	
- - -	- -	Increments 1dB per step	
11000	18h	-12dB	
11001 to 11111	19h to 1Fh	Reserved	

Table 3: Equalizer Gains

4.7 3D Stereo Enhancement

NAU8401 includes digital circuitry to provide flexible 3D enhancement to increase the perceived separation between the right and left channels, and has multiple options for optimum acoustic performance. The equalizer is grouped with the 3D Stereo Enhancement signal processing function. Both functions may be assigned jointly to support the DAC audio output path, or may be jointly disabled from the DAC audio output path.

Registers that affect operation of 3D Stereo Enhancement are:

R18 Enable / Disable 3D enhancement function
R41 3D Audio depth enhancement setting

The amount of 3D enhancement applied can be programmed from the default 0% (no 3D effect) to 100% in register 41, bits 0 to 3 (DEPTH3D), as shown in the following table. Note: 3D enhancement uses increased gain to achieve its effect, so that the source signal may need to be attenuated by up to 6dB to avoid clipping distortion.

Register 41 Bits 0 to 3 3DDEPTH	**3D Effect**
0000	0%
0001	6.7%dB
0010	13.4%dB
- - -	Increments 6.67% for each binary step in the input word
1110	93.3%
1111	100%

Table 4: 3D Enhancement Depth

4.8 DAC Output A-law and μ-law Expansion

Companding (compression | expansion) is used in digital communication systems to optimize signal-to-noise ratios with reduced data bit rates, using non-linear algorithms. NAU8401 supports the two main telecommunications expansion standards on the DAC path receive side: A-law and μ-law. The A-law algorithm is primarily used in European communication systems and the μ-law algorithm is primarily used by North America, Japan, and Australia. On the sending side of a telecommunications system, audio is converted from a linear dynamic range of approximately 13 bits (μ-law) or 12 bits (A-law) into a compressed 8-bit format using non-linear quantization. The compressed signal is an 8bit word containing sign (1-bit), exponent (3-bits) and mantissa (4-bits). The DAC can then convert the compressed back into the original 13-bit or 12-bit linear audio format.

The register affecting companding operation is:

R5 Enable 8-bit mode, enable DAC expansion

Following are the data compression equations set in the ITU-T G.711 standard and implemented in the NAU8401:

4.8.1 μ law

$F(x) = \ln(1 + \mu|x|) / \ln(1 + \mu)$ $-1 \le x \le 1$

with μ=255 for the U.S. and Japan

4.8.2 A-law

$F(x) = A|x| / (1 + \ln A)$ for $x \le 1/A$

$F(x) = (1 + \ln A|x|) / (1 + \ln A)$ for $1/A \le x \le 1$

with A=87.6 for Europe

The companded signal is an 8-bit word consisting of a sign bit, three bits for the exponent, and four bits for the mantissa. When companding is enabled, the PCM interface must be set to an 8-bit word length. When in 8-bit mode, the Register 4 word length control (WLEN) is ignored.

Companding Mode	Register 5			
	Bit 4	Bit3	Bit 2	Bit 1
No Companding (default)	0	0	0	0
DAC				
A-law	1	1		
μ-law	1	0		

Table 5: Companding Control

4.9 8-bit Word Length

Writing a 1 to register 5, bit 5 (CMB8), will cause the PCM interface to use 8-bit word length for data transfer, overriding the word length configuration setting in WLEN (register 4, bits 5 and 6.).

5 Analog Outputs

The NAU8401 features six different analog outputs. These are highly flexible and may be used individually or in pairs for many purposes. However, they are grouped in pairs and named for their most commonly used stereo application end uses. The following sections detail key features and functions of each type of output. Included is a description of the associated output mixers. These mixers are separate internal functional blocks that are important toward understanding all aspects of the analog output section.

Important: For analog outputs depopping purpose, when powering up speakers, headphone, AUXOUTs, certain delays are generated after enabling sequence. However, the delays are created by MCLK and sample rate register. For correct operation, sending I2S signal no earlier than 250ms after speaker or headphone enabled and MCLK appearing.

5.1 Main Mixers (LMAIN MIX and RMAIN MIX)

Each left and right channel is supported by an independent main mixer. This mixer combines signals from a various available signal sources internal to the device. Each mixer may also be selectively enabled/disabled as part of the power management features. The outputs of these mixers are the only signal source for the headphone outputs, and the primary signal source for the loudspeaker outputs.

Each mixer can accept either or both the left and right digital to analog (DAC) outputs. Normally, the left and right DAC is mixed into the associated left and right main output mix. This additional capability to mix opposite DAC channels enables switching the left and right DAC outputs to the opposite channel, or mixing together the left and right DAC signals – all without any processor or host intervention and processing overhead.

Each mixer also can also combine signals directly from the respective left or right line input (LINPUT and RINPUT). Each of these analog input paths may be muted, or have an applied selectable gain between -15dB and +6dB in 3dB steps.

Registers that affect operation of the Main Mixers are:

R3 Power control for the left and right main mixer
R49 left and right DAC cross-mixing source selection options
R50 left DAC to left main mixer source selection option
R51 right DAC to right main mixer source selection option
R50 left mixer source select, and gain settings
R51 right mixer source select, and gain settings

5.2 Auxiliary Mixers (AUX1 MIXER and AUX2 MIXER)

Each auxiliary analog output channel is supported by an independent mixer dedicated to the auxiliary output function. This mixer combines signals from a various available signal sources internal to the device. Each mixer may also be selectively enabled/disabled as part of the power management features.

Unlike the main mixers, the auxiliary mixers are not identical and combine different signal sets internal to the device. These mixers in conjunction with the auxiliary outputs greatly increase the overall capabilities and flexibility of the NAU8401.

The AUX1 mixer combines together any or all of the following:

Left Main Mixer output
Right Main Mixer output
Left DAC output
Right DAC output

The AUX2 mixer combines together any or all of the following:

Left Main Mixer output
Left DAC output
Output from AUX1 mixer stage

Registers that affect operation of the Auxiliary Mixers are:

R1 Power control for the left and right auxiliary mixer
R56 Signal source selection for the AUX2 mixer
R57 Signal source selection for the AUX1 mixer

5.3 Right Speaker Submixer

The right speaker submixer serves two important functions. One is to optionally invert the output from the Right Main Mixer as an optional signal source for the right channel loudspeaker output driver. This inversion is normal and necessary in typical applications using the loudspeaker drivers.

The other function of the right speaker submixer is to mix the RINPUT input signal directly into the right channel speaker output driver. This enables the RINPUT signal to be output on the right loudspeaker channel, but not be mixed to any other output. The traditional purpose of this path is to support an old-style beep sound, such as traditionally generated by a microprocessor output toggle bit. On the NAU8401, this traditional function is supported by a full quality signal path that may be used for any purpose. The volume for this path has a selectable gain from -15dB through +6dB in 3dB step increments.

There is no separate power management control feature for the Right Speaker Submixer. The register that affects the Right Speaker Submixer is:

R43 Input mute controls, volume for RINPUT path

5.4 Headphone Outputs (LHP and RHP)

These are high quality, high current output drivers intended for driving low impedance loads such as headphones, but also suitable for a wide range of audio output applications. The only signal source for each of these outputs is from the associated left and right Main Mixer. Power for this section is provided from the VDDA pin. Each driver may be selectively enabled/disabled as part of the power management features.

Each output can be individually muted, or controlled over a gain range of -57dB through +6dB in 3dB steps. Gain changes for the two headphone outputs can be coordinated through use of an update bit feature as part of the register controls. Additionally, clicks that could result from gain changes can be suppressed using an optional zero crossing feature.

Registers that affect the headphone outputs are:

R2 Power management control for the left and right headphone amplifier
R52 Volume, mute, update, and zero crossing controls for left headphone driver
R53 Volume, mute, update, and zero crossing controls for right headphone driver

Important: The R52 and R53 update bits are write-only bits. The primary intended purpose of the update bit is to enable simultaneous changes to both the left and right headphone output volume values, even though these two register values must be written sequentially. When there is a write operation to either R52 or R53 volume settings, but the update bit is not set (value = 0), the new volume setting is stored as pending for the future, but does not go into effect. When there is a write operation to either R52 or R53 and the update bit is set (value = 1), then the new value in the register being written is immediately put into effect, and any pending value in the other headphone output volume register is put into effect at the same time.

Zero-Crossing controls are implemented to suppress clicking sounds that may occur when volume setting changes take place while an audio input signal is active. When the zero crossing function is enabled (logic = 1), any volume change for the affected channel will not take place until the audio input signal passes through the zero point in its peak-to-peak swing. This prevents any instantaneous voltage change to the audio signal caused by volume setting changes. If the zero crossing function is disabled (logic = 0), volume changes take place instantly on condition of the Update Bit, but without regard to the instantaneous voltage level of the affected audio input signal.

5.5 Speaker Outputs

These are high current outputs suitable for driving low impedance loads, such as an 8-ohm loudspeaker. Both outputs may be used separately for a wide range of applications, however, the intended application is to use both outputs together in a BTL (Bridge-Tied-Load, and also, Balanced-Transformer-Less) configuration. In most applications, this configuration requires an additional signal inversion, which is a feature supported in the right speaker submixer block.
This inversion is normal and necessary when the two speaker outputs are used together in a BTL (Bridge-Tied-Load, and also, Balanced-Transformer-Less) configuration. In this physical configuration, the RSPKOUT signal is connected to one pole of the loudspeaker, and the LSPKOUT signal is connected to the other pole of the loudspeaker. Mathematically, this creates within the loudspeaker a signal equal to (Left-Right). The desired mathematical operation for a stereo signal is to drive the speaker with (Left+Right). This is accomplished by implementing an additional inversion to the right channel signal. For most applications, best performance will be achieved when care is taken to insure that all gain and filter settings in both the left and right channel paths to the loudspeaker drivers are identical.

Power for the loudspeaker outputs is supplied via the VDDSPK pin, and ground is independently provided as the VSSPK pin. This power option enables an operating voltage as high as 5Vdc and helps in a system design to prevent high current outputs from creating noise on other supply voltage rails or system grounds. VSSPK must be connected at some point in the system to VSSA, but provision of the VSSPK as a separate high current ground pin facilitates managing the flow of current to prevent “ground bounce” and other ground noise related problems.

Each loudspeaker output may be selectively enabled/disabled as part of the power management features. Registers that affect the loudspeaker outputs are:

R3 Power management control of LSPKOUT and RSPKOUT driver outputs
R3 Speaker bias control (BIASGEN) set logic = 1 for maximum power and VDDSPK > 3.60Vdc
R48 Driver distortion mode control
R49 Disable boost control for speaker outputs for VDDSPK 3.3V or lower
R54 Volume (gain), mute, update bit, and zero crossing control for left speaker driver
R55 Volume (gain), mute, update bit, and zero crossing control for right speaker driver

Important: The R49 boost control option is set in the power-on reset condition for high voltage operation of VDDSPK. If VDDSPK is greater than 3.6Vdc, the R49 boost control bits should be remain at the power-on default settings. This insures reliable operation of the part, proper DC biasing, and optimum scaling of the signal to enable the output to achieve full scale output when VDDSPK is greater than VDDA. In the boost mode, the gain of the output stage is increased by a factor of 1.5 times the normal gain value.

Important: The R54 and R55 update bits are write-only bits. The primary intended purpose of the update bit is to enable simultaneous changes to both the left and right headphone output volume values, even though these two register values must be written sequentially. When there is a write operation to either R54 or R55 volume settings, but the update bit is not set (value = 0), the new volume setting is stored as pending for the future, but does not go into effect. When there is a write operation to either R54 or R55 and the update bit is set (value = 1), then the new value in the register being written is immediately put into effect, and any pending value in the other headphone output volume register is put into effect at the same time.

Zero-Crossing controls are implemented to suppress clicking sounds that may occur when volume setting changes take place while an audio input signal is active. When the zero crossing function is enabled (logic = 1), any volume change for the affected channel will not take place until the audio input signal passes through the zero point in its peak-to-peak swing. This prevents any instantaneous voltage change to the audio signal caused by volume setting changes. If the zero crossing function is disabled (logic = 0), volume changes take place instantly on condition of the Update Bit, but without regard to the instantaneous voltage level of the affected audio input signal.

The loudspeaker drivers may optionally be operated in an ultralow distortion mode. This mode may require additional external passive components to insure stable operation in some system configurations. No external components are required in normal mode speaker driver operation. Distortion performance in normal operation is excellent, and already suitable for almost every application.

5.6 Auxiliary Outputs

These are high current outputs suitable for driving low impedance loads such as headphones or line level loads. Power for these outputs is supplied via the VDDSPK pin, and ground is also independently provided as the VSSPK pin. This power option enables an operating voltage as high as 5Vdc and helps in a system design to prevent high current outputs from creating noise on other supply voltage rails or system grounds. VSSPK must be connected at some point in the system to VSSA, but provision of the VSSPK as a separate high current ground pin facilitates managing the flow of current to prevent "ground bounce" and other ground noise related problems.

Each auxiliary output driver may be selectively enabled/disabled as part of the power management features. Registers that affect the auxiliary outputs are:

R3 Power management control of AUXOUT1 and AUXOUT2 outputs
R3 Speaker bias control (BIASGEN) set logic = 1 for maximum power and VDDSPK > 3.60Vdc
R49 Disable boost control for AUXOUT1 and AUXOUT2 for VDDSPK 3.3Vdc or lower
R56 Mute, gain control, and input selection controls for AUXOUT2
R57 Mute, gain control, and input selection controls for AUXOUT1

Important: The R49 boost control option is set in the power-on reset condition for high voltage operation of VDDSPK. If VDDSPK is greater than 3.6Vdc, the R49 boost control bits should be remain at the power-on default settings. This insures reliable operation of the part, proper DC biasing, and optimum scaling of the signal to enable the output to achieve full scale output when VDDSPK is greater than VDDA. In the boost mode, the gain of the output stage is increased by a factor of 1.5 times the normal gain value.

An optional alternative function for these outputs is to provide a virtual ground for an external headphone device. This is for eliminating output capacitors for the headphone amplifier circuit in applications where this type of design is appropriate. In this type of application, the AUXOUT output is typically operated in the muted condition. In the muted condition, and with the output configured in the non-boost mode (also requiring that VDDSPK < 3.61Vdc), the AUXOUT output DC level will remain at the internal VREF level. This the same internal DC level as used by the headphone outputs. Because these DC levels are nominally the same, DC current flowing through the headphone in this mode of operation is minimized. Depending on the application, one or both of the auxiliary outputs may be used in this fashion.

6 Miscellaneous Functions

6.1 Slow Timer Clock

An internal Slow Timer Clock is supplied to automatically control features that happen over a relatively periods of time, or time-spans. This enables the NAU8401 to implement long time-span features without any host/processor management or intervention.

Two features are supported by the Slow Timer Clock. These are an optional automatic time out for the zero-crossing holdoff of PGA volume changes, and timing for debouncing of the mechanical jack detection feature. If either feature is required, the Slow Timer Clock must be enabled.

The Slow Timer Clock is initialized in the disabled state. The Slow Timer Clock is controlled by only the following register:

R7 Sample rate indication select, and Slow Timer Clock enable

The Slow Timer Clock rate is derived from MCLK using an integer divider that is compensated for the sample rate as indicated by the R7 sample rate register. If the sample rate register value precisely matches the actual sample rate, then the internal Slow Timer Clock rate will be a constant value of 128ms. If the actual sample rate is, for example, 44.1kHz and the sample rate selected in R7 is 48kHz, the rate of the Slow Timer Clock will be approximately 10% slower in direct proportion of the actual vs. indicated sample rate. This scale of difference should not be important in relation to the dedicated end uses of the Slow Timer Clock.

6.2 General Purpose Inputs and Outputs (GPIO1, GPIO2, GPIO3) and Jack Detection

Three pins are provided in the NAU8401 that may be used for limited logic input/output functions. GPIO1 has multiple possible functions, and may be either a logic input or logic output. GPIO2 or GPIO3 may be used as logic inputs dedicated to the purpose of jack detection. GPIO3 is used as a logic output in 4-wire SPI mode, and GPIO2 does not have any logic output capability. Only one GPIO can be selected for jack detection.

If a GPIO is selected for the jack detection feature, the Slow Timer Clock must be enabled. The jack detection function is automatically "debounced" such that momentary changes to the logic value of this input pin are ignored. The Slow Timer Clock is necessary for the debouncing feature.

Registers that control the GPIO functionality are:

R8 GPIO functional selection options
R9 Jack Detection feature input selection and functional options

If a GPIO is selected for the jack detection function, the required Slow Timer Clock determines the duration of the time windows for the input logic debouncing function. Because the logic level changes happen asynchronously to the Slow Timer Clock, there is inherently some variability in the timing for the jack detection function. A continuous and persistent logic change on the GPIO pin used for jack detection will result in a valid internal output signal within 2.5 to 3.5 periods of the Slow Timer Clock. Any logic change of shorter duration will be ignored.

The threshold voltage for a jack detection logic-low level is no higher than 1.0Vdc. The threshold voltage for a jack detection logic-high level is no lower than 1.7Vdc. These levels will be reduced as the VDDC core logic voltage pin is reduced below 1.9Vdc.

6.3 Automated Features Linked to Jack Detection

Some functionality can be automatically controlled by the jack detection logic. This feature can be used to enable the internal analog amplifier bias voltage generator, and/or enable analog output drivers automatically as a result of detecting a logic change at a GPIO pin assigned to the purpose of jack detection. This eliminates any requirement for the host/processor to perform these functions.

The internal analog amplifier bias generator creates the VREF voltage reference and bias voltage used by the analog amplifiers. The ability to control it is a power management feature. This is implemented as a logical "OR" function of either the debounced internal jack detection signal, or the ABIASEN control bit in Register 1. The bias generator will be powered if either of these control signals is enabled (value = 1).

Power management control of four different outputs is also optionally and selectively subject to control linked with the jack detection signal. The four outputs that can be controlled this way are the headphone driver signal pair, loudspeaker driver signal pair, AUXOUT1, and AUXOUT2. Register settings determine which outputs may be enabled, and whether they are enabled by a logic 1 or logic 0 value. Output control is a logical "AND" operation of the jack detection controls, and of the register control bits that normally control the outputs. Both controls must be in the "ON" condition for a given output to be enabled.

Registers that affect these functions are:

R9 GPIO pin selection for jack detect function, jack detection enable, VREF jack enable
R13 bit mapped selection of which outputs are to be enabled when jack detect is in a logic 1 state
R13 bit mapped selection of which outputs are to be enabled when jack detect is in a logic 0 state

7 Clock Selection and Generation

The NAU8401 has two basic clock modes that support the DAC data converters. It can accept external clocks in the slave mode, or in the master mode, it can generate the required clocks from an external reference frequency using an internal PLL (Phase Locked Loop). The internal PLL is a fractional type scaling PLL, and therefore, a very wide range of external reference frequencies can be used to create accurate audio sample rates.

Separate from this DAC clock subsystem, audio data are clocked to and from the NAU8401 by means of the control logic described in the Digital Audio Interfaces section. The audio bit rate and audio sample rate for this data flow are managed by the Frame Sync (FS) and Bit Clock (BCLK) pins in the Digital Audio Interface.

It is important to understand that the sampling rate for the DAC data converters is not determined by the Digital Audio Interface, and instead, this rate is derived exclusively from the Internal Master Clock (IMCLK). It is therefore a requirement that the Digital Audio Interface and data converters be operated synchronously, and that the FS, BCLK, and IMCLK signals are all derived from a common reference frequency. If these three clocks signals are not synchronous, audio quality will be reduced.

The IMCLK is always exactly 256 times the sampling rate of the data converters.

IMCLK is output from the Master Clock Prescaler. The prescaler reduces by an integer division factor the input frequency input clock. The source of this input frequency clock is either the external MCLK pin, or the output from the internal PLL Block.

Registers that are used to manage and control the clock subsystem are:

R1 Power management, enable control for PLL (default = disabled)
R6 Master/slave mode, clock scaling, clock selection
R7 Sample rate indication (scales DSP coefficients and timing – does NOT affect actual sample rate
R8 MUX control and division factor for PLL output on GPIO1
R36 PLL Prescaler, Integer portion of PLL frequency multiplier
R37 Highest order bits of 24-bit fraction of PLL frequency multiplier
R38 Middle order bits of 24-bit fraction of PLL frequency multiplier
R39 Lowest order bits of 24-bit fraction of PLL frequency multiplier

In Master Mode, the IMCLK signal is used to generate FS and BCLK signals that are driven onto the FS and BCLK pins and input to the Digital Audio Interface. FS is always IMCLK/256 and the duty cycle of FS is automatically adjusted to be correct for the mode selected in the Digital Audio Interface. The frequency of BCLK may optionally be divided to optimize the bit clock rate for the application scenario.

In Slave Mode, there is no connection between IMCLK and the FS and BCLK pins. In this mode, FS and BLCK are strictly input pins, and it is the responsibility of the system designer to insure that FS, BCLK, and IMCLK are synchronous and scaled appropriately for the application.

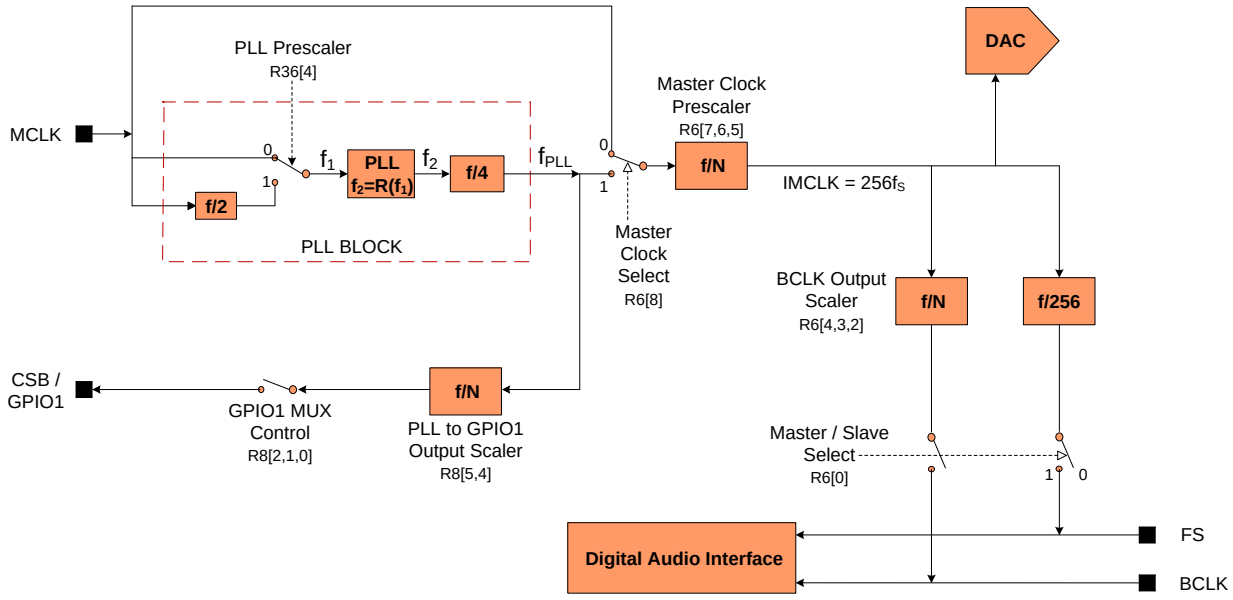


Figure 5: PLL and Clock Select Circuit

7.1 Phase Locked Loop (PLL) General Description

The PLL may be optionally used to multiply an external input clock reference frequency by a high resolution fractional number. To enable the use of the widest possible range of external reference clocks, the PLL block includes an optional divide-by-two prescaler for the input clock, a fixed divide-by-four scaler on the PLL output, and an additional programmable integer divider that is the Master Clock Prescaler.

The high resolution fraction for the PLL is the ratio of the desired PLL oscillator frequency (f_2), and the reference frequency at the PLL input (f_1). This can be represented as $R = f_2/f_1$, with R in the form of a decimal number: xy.abcdefgh. To program the NAU8401, this value is separated into an integer portion ("xy"), and a fractional portion, "abcdefgh". The fractional portion of the multiplier is a value that when represented as a 24-bit binary number (stored in three 9-bit registers on the NAU8401), very closely matches the exact desired multiplier factor.

To keep the PLL within its optimal operating range, the integer portion of the decimal number ("xy"), must be any of the following decimal values: 6, 7, 8, 9, 10, 11, or 12. The input and output dividers outside of the PLL are often helpful to scale frequencies as needed to keep the "xy" value within the required range. Also, the optimum PLL oscillator frequency is in the range between 90MHz and 100MHz, and thus, it is best to keep f_2 within this range.

In summary, for any given design, choose:

- IMCLK = desired Master Clock = (256)*(desired codec sample rate)
- f_2 = (4)*(P)(IMCLK), where P is the Master Clock Prescale integer value; optimal f_2: 90MHz< f_2 <100MHz
- f_1 = (MCLK)/(D), where D is the PLL Prescale factor of 1, or 2, and MCLK is the frequency at the MCLK pin
  note: The integer values for D and P are chosen to keep the PLL in its optimal operating range. It may be best to assign initial values of 1 to both D and P, and then by inspection, determine if they should be a different value.
- $R = f_2/f_1$ = xy.abcdefgh decimal value, which is the fractional frequency multiplication factor for the PLL
- N = xy truncated integer portion of the R value, and limited to decimal value 6, 7, 8, 9, 10, 11, or 12
- $K = (2^{24})*(0.abcdefgh)$, rounded to the nearest whole integer value, then converted to a binary 24-bit value
- R36 is set with the whole number integer portion, N, of the multiplier
- R37, R38, R39 are set collectively with the 24-bit binary fractional portion, K, of the multiplier
- R36 PLL Prescaler set as necessary
- R6 Master Clock Prescaler and BCLK Output Scaler set as necessary

7.1.1 Phase Locked Loop (PLL) Design Example

In an example application, a desired sample rate for the DAC is known to be 48.000kHz. Therefore, it is also known that the IMCLK rate will be 256fs, or 12.288MHz. Because there is a fixed divide-by-four scaler on the PLL output, then the desired PLL oscillator output frequency will be 49.152MHz.

In this example system design, there is already an available 12.000MHz clock from the USB subystem. To reduce system cost, this clock will also be used for audio. Therefore, to use the 12MHz clock for audio, the desired fractional multiplier ratio would be R = 49.152/12.000 = 4.096. This value, however, does not meet the requirement that the "xy" whole number portion of the multiplier be in the inclusive range between 6 and 12. To meet the requirement, the Master Clock Prescaler can be set for an additional divide-by-two factor. This now makes the PLL required oscillator frequency 98.304 MHz, and the improved multiplier value is now R = 98.304/12.000 = 8.192.

To complete this portion of the design example, the integer portion of the multiplier is truncated to the value, 8. The fractional portion is multiplied by 2^{24}, as to create the needed 24-bit binary fractional value. The calculation for this is: $(2^{24})(0.192) = 3221225.472$. It is best to round this value to the nearest whole value of 3221225, or hexadecimal 0x3126E9. Thus, the values to be programmed to set the PLL multiplier whole number integer and fraction are:

```
R36  0xnm8   ; integer portion of fraction,  (nm represents other settings in R36)
R37  0x00C   ; highest order 6-bits of 24-bit fraction
R38  0x093   ; middle 9-bits of 24-bit fraction
R39  0x0E9   ; lowest order 9-bits of 24-bit fraction
```

Below are additional examples of results for this calculation applied to commonly available clock frequencies and desired IMCLK 256fs sample rates.

MCLK (MHz)	Desired 256fs IMCLK rate (MHz)	PLL oscillator f_2 (MHz)	PLL Prescaler divider	Master Clock divider	Fractional Multiplier R = f_2/f_1	Integer Portion N (Hex)	Fractional Portion K (Hex)
12.0	11.28960	90.3168	1	2	7.526400	7	86C226
12.0	12.28800	98.3040	1	2	8.192000	8	3126E9
14.4	11.28960	90.3168	1	2	6.272000	6	45A1CA
14.4	12.28800	98.3040	1	2	6.826667	6	D3A06D
19.2	11.28960	90.3168	2	2	9.408000	9	6872B0
19.2	12.28800	98.3040	2	2	10.240000	A	3D70A3
19.8	11.28960	90.3168	2	2	9.122909	9	1F76F8
19.8	12.28800	98.3040	2	2	9.929697	9	EE009E
24.0	11.28960	90.3168	2	2	7.526400	7	86C226
24.0	12.28800	98.3040	2	2	8.192000	8	3126E9
26.0	11.28960	90.3168	2	2	6.947446	6	F28BD4
26.0	12.28800	98.3040	2	2	7.561846	7	8FD526

Table 6: PLL Frequency Examples

7.2 CSB/GPIO1 as PLL output

CSB/GPIO1 is a multi-function pin that may be used for a variety of purposes. If not required for some other purpose, this pin may be configured to output the clock frequency from the PLL subsystem. This is the same frequency that is available from the PLL subsystem as the input to the Master Clock Prescaler. This frequency may be optionally divided by an additional integer factor of 2, 3, or 4, before being output on GPIO1.

8 Control Interfaces

8.1 Software Reset

The entire NAU8401 and all of its control registers can be reset to default initial conditions by writing any value to Register 0, using any of the control interface modes. Writing to any other valid register address terminates the reset condition, but all registers will now be set to their power-on default values.

8.2 Selection of Control Mode

The NAU8401 features include a serial control bus that provides access to all of the device control registers. This bus may be configured either as a 2-wire interface that is interoperable with industry standard implementations of the the I2C serial bus, or as a 3-wire/4-wire bus compatible with commonly used industry implementations of the SPI (Serial Peripheral Interface) bus.

Mode selection is accomplished by means of combination of the MODE control logic pin, and the SPIEN control bit in Register 7. The following table shows the three functionally different modes that are supported.

MODE Pin	SPIEN bit R7[8]	Description
0	0	2-Wire Interface, Read/Write operation
1	X "don't care"	SPI Interface 3-Wire Write-only operation
0	1	SPI Interface 4-Wire Read operation SPI Interface 4-Wire Write operation

Table 7: Control Interface Selection

The timing in all three bus configurations is fully static. This results in good compatibility with standard bus interfaces, and also, with software simulated buses. A software simulated bus can be very simple and low cost, such as by utilizing general purpose I/O pins on the host controller and software "bit banging" techniques to create the required timing.

8.3 2-Wire-Serial Control Mode (I^2C Style Interface)

The 2-wire bus is a bidirectional serial bus protocol. This protocol defines any device that sends data onto the bus as a transmitter (or master), and the receiving device as the receiver (or slave). The NAU8401 can function only as a slave device when in the 2-wire interface configuration.

8.4 2-Wire Protocol Convention

All 2-Wire interface operations must begin with a START condition, which is a HIGH-to-LOW transition of SDIO while SCLK is HIGH. All 2-Wire interface operations are terminated by a STOP condition, which is a LOW to HIGH transition of SDIO while SCLK is HIGH. A STOP condition at the end of a read or write operation places the device in a standby mode.

An acknowledge (ACK), is a software convention is used to indicate a successful data transfer. To allow for the ACK response, the transmitting device releases the SDIO bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDIO line LOW to acknowledge the reception of the eight bits of data.

Following a START condition, the master must output a device address byte. This consists of a 7-bit device address, and the LSB of the device address byte is the R/W (Read/Write) control bit. When R/W=1, this indicates the master is initiating a read operation from the slave device, and when R/W=0, the master is initiating a write operation to the slave device. If the device address matches the address of the slave device, the slave will output an ACK during the period when the master allows for the ACK signal.

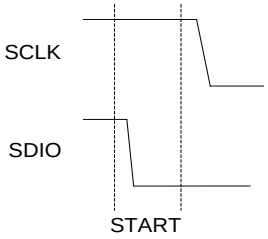


Figure 6: Valid START Condition

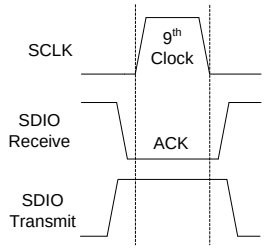


Figure 7: Valid Acknowledge

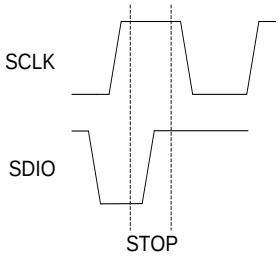


Figure 8: Valid STOP Condition

0	0	1	1	0	1	0	R/W	Device Address Byte
A7	A6	A5	A4	A3	A2	A1	A0	Control Address Byte
D7	D6	D5	D4	D3	D2	D1	D0	Data Byte

Figure 9: Slave Address Byte, Control Address Byte, and Data Byte

8.5 2-Wire Write Operation

A Write operation consists of a two-byte instruction followed by one or more Data Bytes. A Write operation requires a START condition, followed by a valid device address byte with R/W=0, a valid control address byte, data byte(s), and a STOP condition.

The NAU8401 is permanently programmed with “0011010” as the Device Address. If the Device Address matches this value, the NAU8401 will respond with the expected ACK signaling as it accepts the data being transmitted into it.

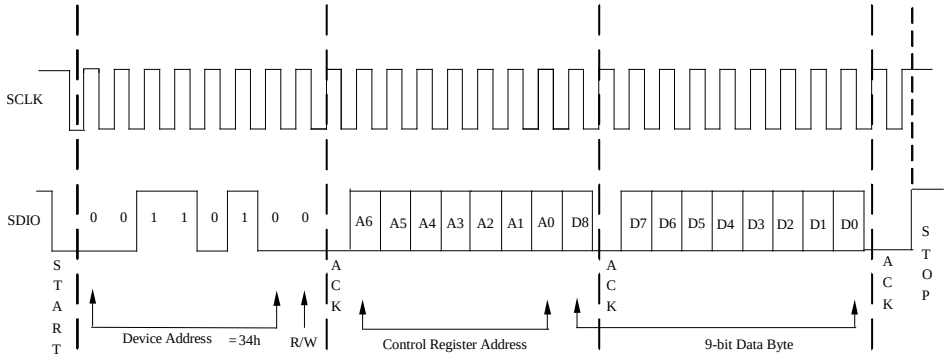


Figure 10: Byte Write Sequence

8.6 2-Wire Read Operation

A Read operation consists of a three-byte Write instruction followed by a Read instruction of one or more data bytes. The bus master initiates the operation issuing the following sequence: a START condition, device address byte with the R/W bit set to "0", and a Control Register Address byte. This indicates to the slave device which of its control registers is to be accessed.

The NAU8401 is permanently programmed with "0011010" as its device address. If the device address matches this value, the NAU8401 will respond with the expected ACK signaling as it accepts the Control Register Address being transmitted into it. After this, the master transmits a second START condition, and a second instantiation of the same device address, but now with R/W=1.

After again recognizing its device address, the NAU8401 transmits an ACK, followed by a two byte value containing the nine bits of data from the selected control register inside the NAU8401. Unused bits in the byte containing the MSB information from the NAU8401 are output by the NAU8401 as zeros.

During this phase, the master generates the ACK signaling with each byte transferred from the NAU8401. If there is no STOP signal from the master, the NAU8401 will internally auto-increment the target Control Register Address and then output the two data bytes for this next register in the sequence.

This process will continue as long as the master continues to issue ACK signaling. If the Control Register Address being indexed inside the NAU8401 reaches the value 0x7F (hexadecimal) and the value for this register is output, the index will roll over to 0x00. The data bytes will continue to be output until the master terminates the read operation by issuing a STOP condition.

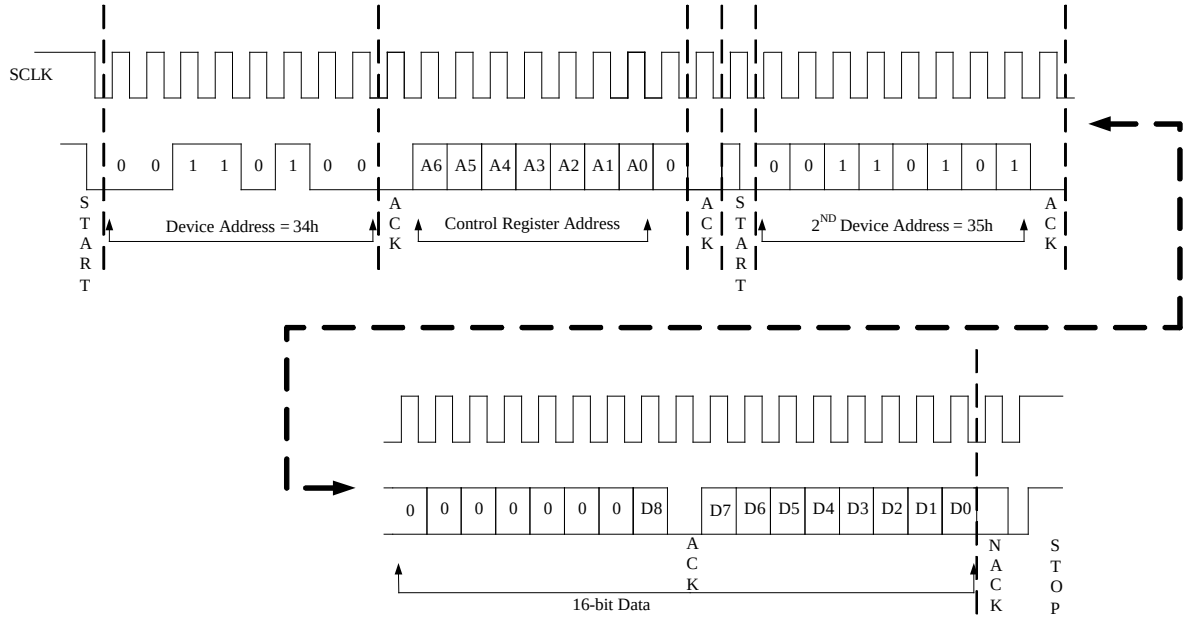


Figure 11: Read Sequence

8.7 SPI Control Interface Modes

The Serial Peripheral Interface (SPI) is a widely utilized interface protocol, and the NAU8401 supports two modes of SPI operation. When the MODE pin on the NAU8401 is in a logic HIGH condition, the device operates in the SPI 3-wire Write Mode. This is a write-only mode with a 16-bit transaction size. If the MODE pin is in a logic LOW condition, and the SPIEN control bit is set in Register 5, the SPI 4-wire Read/Write modes are enabled.

8.8 SPI 3-Wire Write Operation

Whenever the MODE pin on the NAU8401 is in the logic HIGH condition, the device control interface will operate in the 3-Wire Write mode. This is a write-only mode that does not require the fourth wire normally used to read data from a device on an SPI bus implementation. This mode is a 16-bit transaction consisting of a 7-bit Control Register Address, and 9-bits of control register data. In this mode, SDIO data bits are clocked continuously into a temporary holding register on each rising edge of SCLK, until the CSB pin undergoes a LOW-to-HIGH logic transition. At the time of the transition, the most recent 16-bits of data are latched into the NAU8401, with the 9-bit data value being written into the NAU8401 control register addressed by the Control Register Address portion of the 16-bit value.

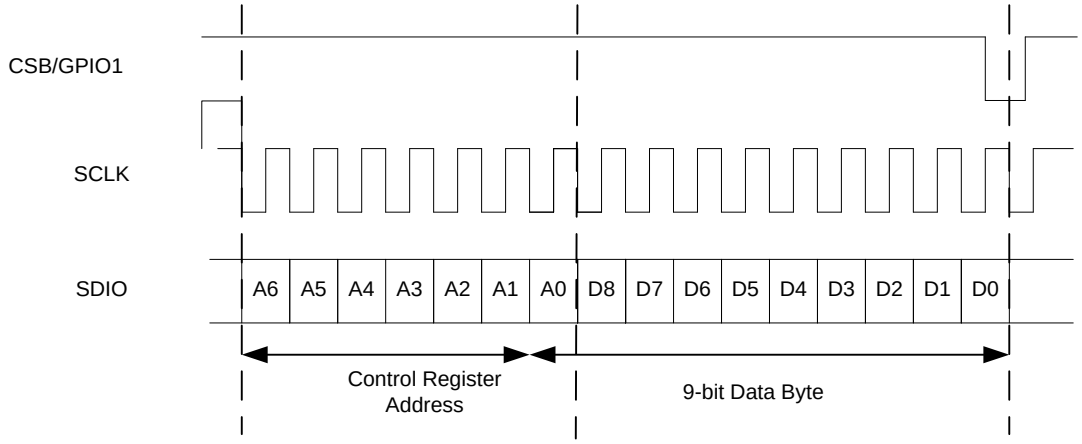


Figure 12: Register write operation using a 16-bit SPI Interface

8.9 SPI 4-Wire 24-bit Write and 32-bit Read Operation

The SPI 4-Wire Read/Write modes are enabled when the NAU8401 MODE pin is in a logic LOW condition, AND when the SPI Enable bit (SPIEN) is set in Register 7, Bit 8. Note that any time after either a hardware reset or software reset of the NAU8401 has occurred, the SPIEN bit must be set before the SPI 4-Wire Read/Write modes can be used. This must be done using either the SPI 3-Wire Write mode, or using the 2-Wire Write operation.

8.10 SPI 4-Wire Write Operation

The SPI 4-Wire write operation is a full SPI data transaction. However, only three wires are needed, as this is a write-only operation with no return data. A fourth wire is needed only when there are bi-directional data. The CSB/GPIO1 pin on the NAU8401 is used as the chip select function in the SPI transaction.

After CSB is held in a logic LOW condition, data bits from SDIO are clocked into the NAU8401 on every rising edge of SCLK. A write operation is indicated by the value 0x10 (hexadecimal) placed in the Device Address byte of the transaction. This byte is followed by a 7-bit Control Register Address and a 9-bit data value packed into the next two bytes of three-byte sequence. After the LSB of the Data Byte is clocked into the NAU8401, the 9-bit data value is automatically transferred into the NAU8401 register addressed by the Control Register Address value.

If only a single register is to be written, CSB/GPIO must be put into a logic HIGH condition after the LSB of the Data Byte is clocked into the device. If CSB/GPIO1 remains in a logic LOW condition, the NAU8401 will auto-index the Control Register Address value to the next higher address, and the next two bytes will be clocked into the next sequential NAU8401 register address. This will continue as long as CSB/GPIO1 is in the logic LOW condition. If the Control Register Address being indexed inside the NAU8401 reaches the value 0x7F (hexadecimal), and after the value for this register is written, the index will roll over to 0x00 and the process will continue.

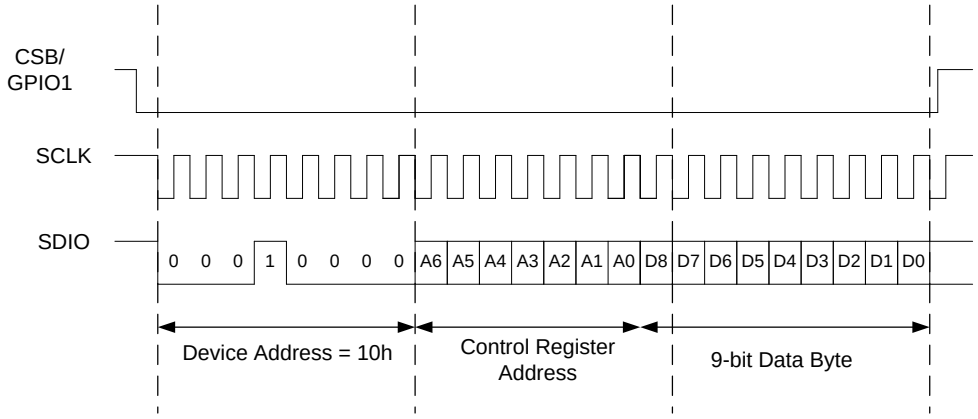


Figure 13: Register Write operation using a 24-bit SPI Interface

8.11 SPI 4-Wire Read Operation

The SPI 4-Wire Read operation is a full SPI data transaction with a two-byte address phase, and two-byte data phase. The CSB/GPIO1 pin on the NAU8401 is used as the chip select function in the SPI transaction.

After CSB is held in a logic LOW condition, data bits from SDIO are clocked into the NAU8401 on every rising edge of SCLK. A read operation is indicated by the value 0x20 (hexadecimal) placed in the Device Address byte of the transaction. This byte is followed by a 7-bit Control Register Address, padded by a non-used zero value in the LSB portion of the Control Register Address.

After the LSB of the Control Register Address is clocked, the NAU8401 will begin outputting its data on the GPIO3 pin, beginning with the very next SCLK rising edge. These data are transmitted in two bytes and contain the 9-bit value from the NAU8401 register selected by the Control Register Address. The data are transmitted MSB first, with the first 7-bits of the two byte value padded by zeros.

If only a single register is to be read, CSB/GPIO must be put into a logic HIGH condition after the LSB of the Data Byte 1 is clocked from the NAU8401. If CSB/GPIO1 remains in a logic LOW condition, the NAU8401 will auto-index the Control Register Address value to the next higher address, and the next two bytes will be clocked from the next sequential NAU8401 register address. This will continue as long as CSB/GPIO1 is in the logic LOW condition. If the Control Register Address being indexed inside the NAU8401 reaches the value 0x7F (hexadecimal), and after the value for this register is output, the index will roll over to 0x00 and the process will continue.

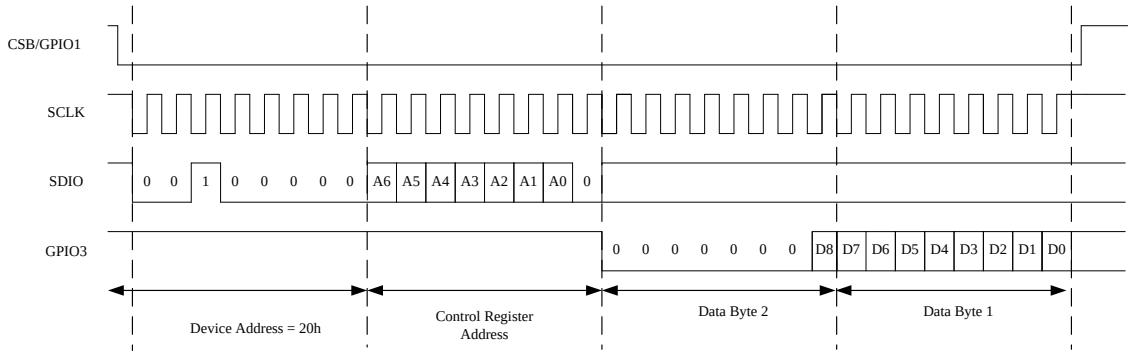


Figure 14: Register Read operation through a 32-bit SPI Interface

9 Digital Audio Interfaces

The NAU8401 can be configured as either the master or the slave, by setting register 6, bit 0, to 1 for master mode and to 0 for slave mode. Slave mode is the default if this bit is not written. In master mode, NAU8401 outputs both Frame Sync (FS) and the audio data bit clock (BCLK,) has full control of the data transfer. In the slave mode, an external controller supplies BCLK and FS. Data for the DAC are latched from the DACIN pin on the rising edge of BCLK.

NAU8401 supports six audio formats as shown below, all with an MSB-first data format. The default mode is I^2S.

PCM Mode	Register 4, bits 3 -4 AIFF	Register 4, bit 7 LRP	Register 60, bit 8 PCMTSEN
Right Justified	00	0	0
Left Justified	01	0	0
I^2S	10	0	0
PCM A	11	0	0
PCM B	11	1	0
PCM Time Slot	11	Don't care	1

Table 8: Digital Audio Interface Modes

9.1 Right-Justified Audio Data

In right-justified mode, the LSB is clocked on the last BCLK rising edge before FS transitions. When FS is HIGH, left channel data is transmitted and when FS is LOW, right channel data is transmitted. This is shown in the figure below.

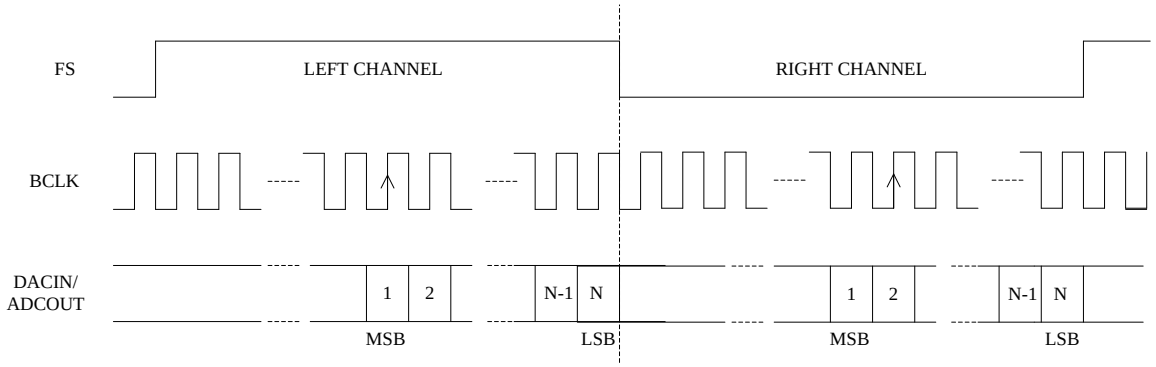


Figure 15: Right-Justified Audio Interface

9.2 Left-Justified Audio Data

In left-justified mode, the MSB is clocked on the first BCLK rising edge after FS transitions. When FS is HIGH, left channel data is transmitted and when FS is LOW, right channel data is transmitted. This is shown in the figure below.

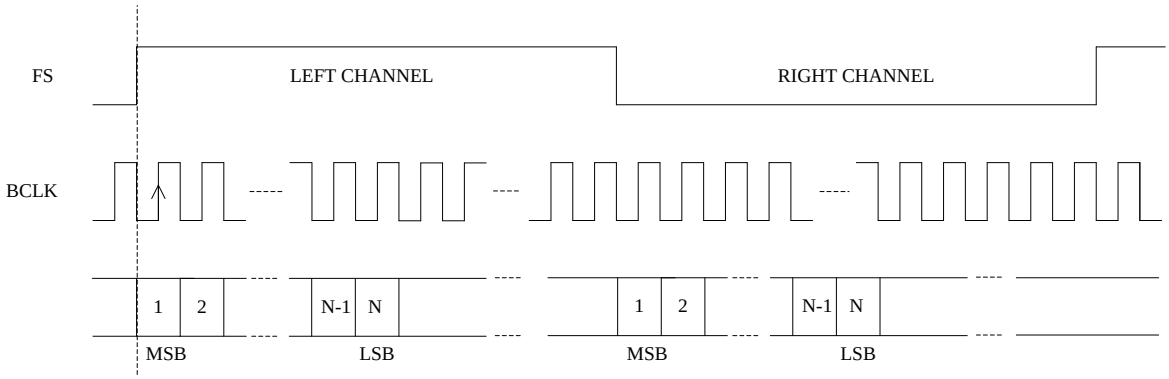


Figure 16: Left-Justified Audio Interface

9.3 I²S Audio Data

In I²S mode, the MSB is clocked on the second BCLK rising edge after FS transitions. When FS is LOW, left channel data is transmitted and when FS is HIGH, right channel data is transmitted. This is shown in the figure below.

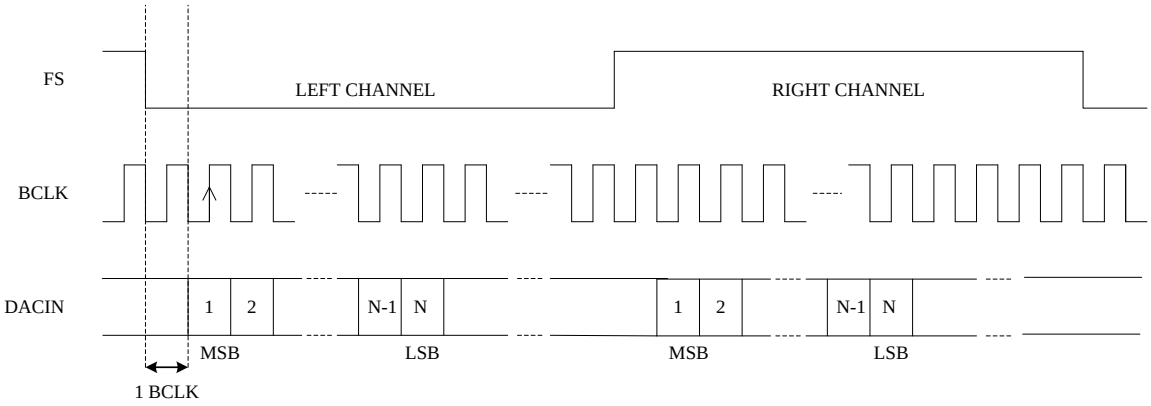


Figure 17: I2S Audio Interface

9.4 PCM A Audio Data

In the PCM A mode, left channel data is transmitted first followed immediately by right channel data. The left channel MSB is clocked on the second BCLK rising edge after the FS pulse rising edge, and the right channel MSB is clocked on the next SCLK after the left channel LSB. This is shown in the figure below.

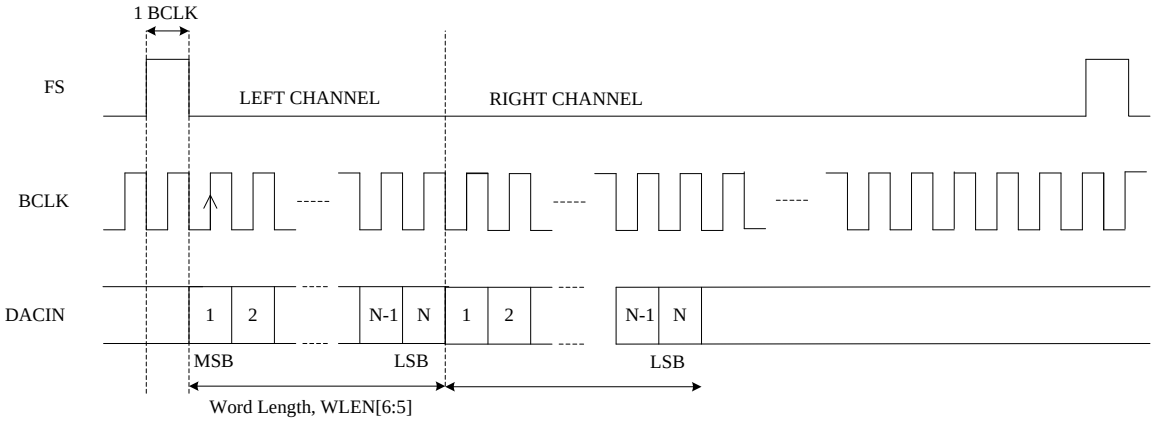


Figure 18: PCM A Audio Interface

9.5 PCM B Audio Data

In the PCM B mode, left channel data is transmitted first followed immediately by right channel data. The left channel MSB is clocked on the first BCLK rising edge after the FS pulse rising edge, and the right channel MSB is clocked on the next SCLK after the left channel LSB. This is shown in the figure below.

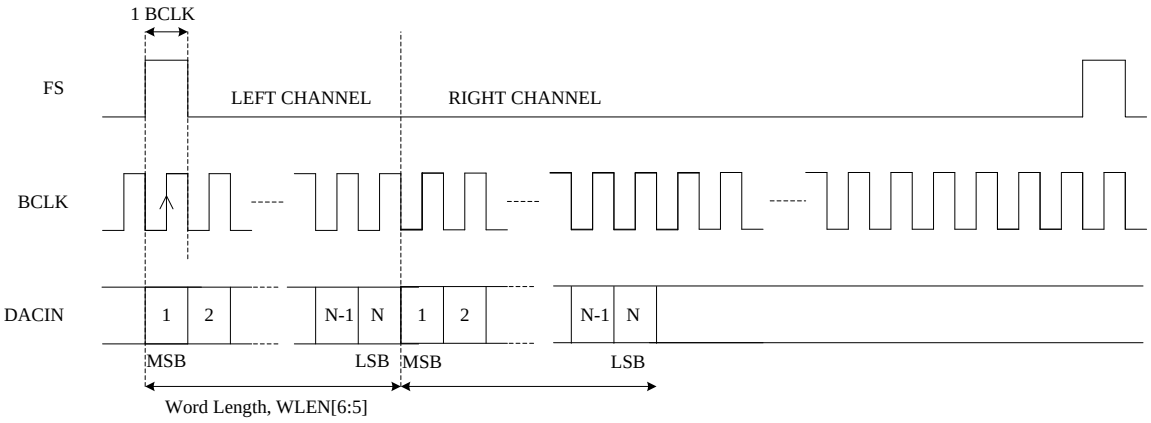


Figure 19: PCM-B Audio Interface

9.6 PCM Time Slot Audio Data

The PCM time slot mode is used to delay the time at which the DAC data are clocked into the device. This increases the flexibility of the NAU8401 to be used in a wide range of system designs. One key application of this feature is to enable multiple NAU8401 or other devices to share the audio data bus, thus enabling more than two channels of audio. This feature may also be used to swap left and right channel data, or to cause both the left and right channels to use the same data.

Normally, the DAC data are clocked immediately after the Frame Sync (FS). In the PCM time slot mode, the audio data are delayed by a delay count specified in the device control registers. The left channel MSB is clocked on the BCLK rising edge defined by the delay count set in Registers 59 and 60. The right channel MSB is clocked on the BCLK rising edge defined by the delay count set in Registers 60 and 61.

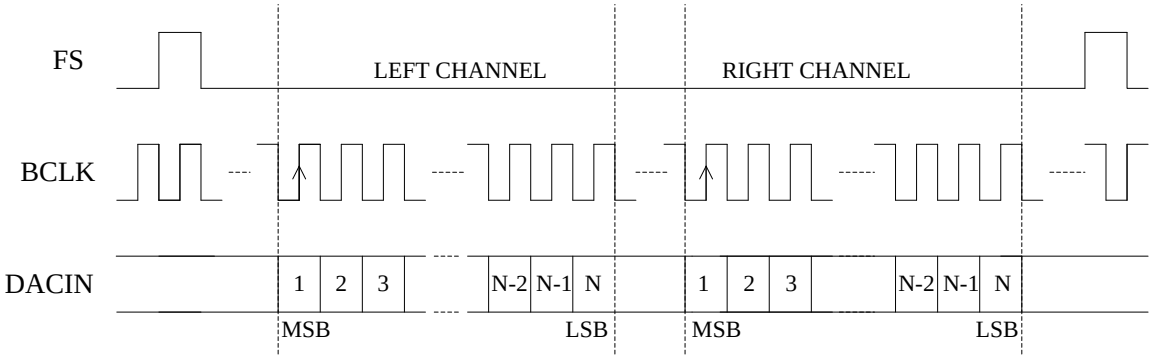


Figure 20: PCM Time Slot Audio Interface

9.7 Control Interface Timing

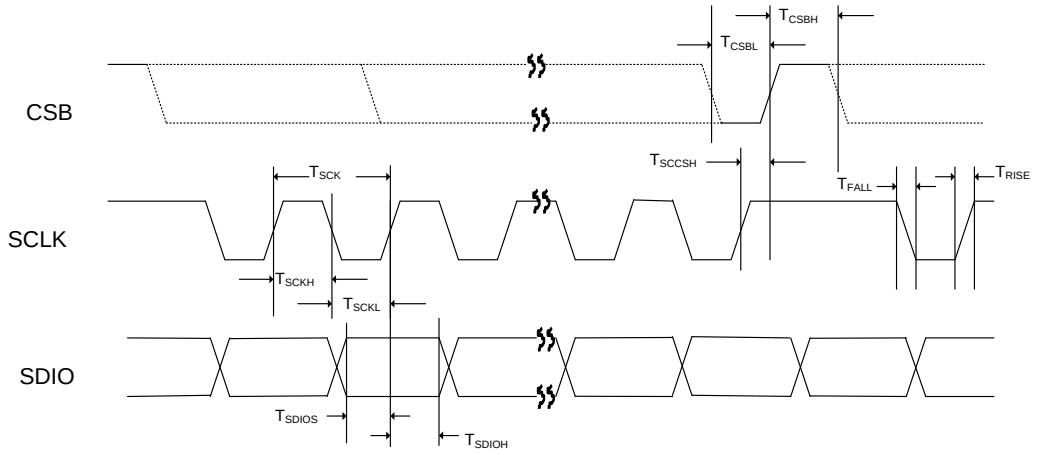


Figure 21: 3-wire Control Mode Timing

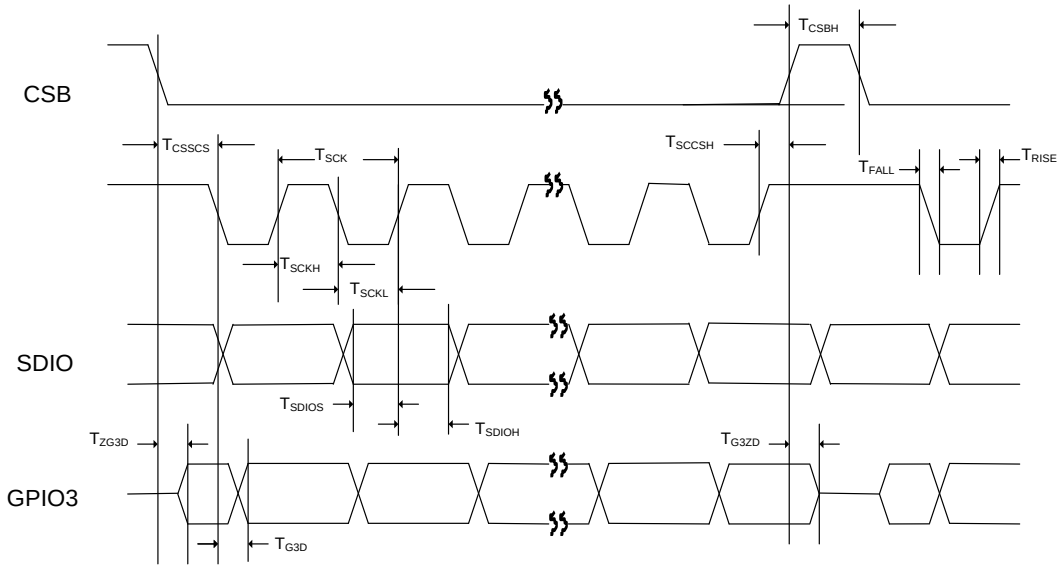


Figure 22: 4-wire Control Mode Timing

Symbol	Description	min	typ	max	unit
T_{SCK}	SCLK Cycle Time	80	-	-	ns
T_{SCKH}	SCLK High Pulse Width	35	-	-	ns
T_{SCKL}	SCLK Low Pulse Width	35	-	-	ns
T_{RISE}	Rise Time for all Control Interface Signals	-	-	10	ns
T_{FALL}	Fall Time for all Control Interface Signals	-	-	10	ns
T_{CSSCS}	CSB Falling Edge to 1st SCLK Falling Edge Setup Time (4 wire Mode Only)	30	-	-	ns
T_{SCCSH}	Last SCLK Rising Edge to CSB Rising Edge Hold Time	30	-	-	ns
T_{CSBL}	CSB Low Time	30	-	-	ns
T_{CSBH}	CSB High Time between CSB Lows	30	-	-	ns
T_{SDIOS}	SDIO to SCLK Rising Edge Setup Time	20	-	-	ns
T_{SDIOH}	SCLK Rising Edge to SDIO Hold Time	20	-	-	ns
T_{ZG3D}	Delay Time from CSB Falling Edge to GPIO3 Active (4 wire Mode Only)	--	--	15	ns
T_{G3ZD}	Delay Time from CSB Rising Edge to GPIO3 Tri-state (4-wire Mode Only)	--	--	15	ns
T_{G3D}	Delay Time from SCLK Falling Edge to GPIO3 (4-wire Mode Only)	-	-	15	ns

Table 9: Three- and Four Wire Control Timing Parameters

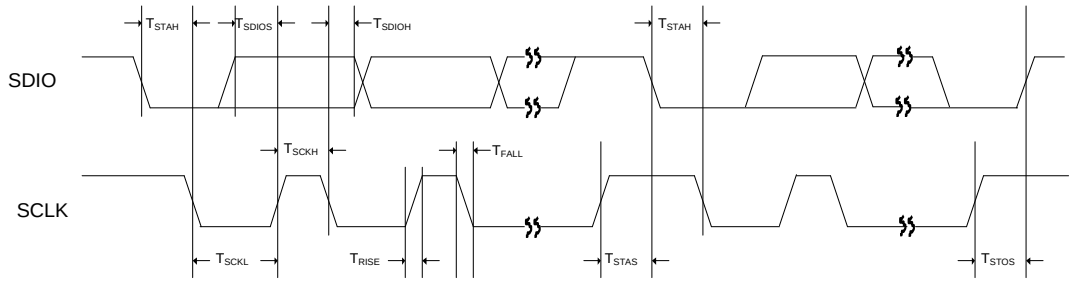


Figure 23: Two-wire Control Mode Timing

Symbol	Description	min	typ	max	unit
T_{STAH}	SCLK falling edge to SDIO falling edge hold timing in START / Repeat START condition	600	-	-	ns
T_{STAS}	SDIO rising edge to SCLK falling edge setup timing in Repeat START condition	600	-	-	ns
T_{STOS}	SDIO rising edge to SCLK rising edge setup timing in STOP condition	600	-	-	ns
T_{SCKH}	SCLK High Pulse Width	600	-	-	ns
T_{SCKL}	SCLK Low Pulse Width	1,300	-	-	ns
T_{RISE}	Rise Time for all 2-wire Mode Signals	-	-	300	ns
T_{FALL}	Fall Time for all 2-wire Mode Signals	-	-	300	ns
T_{SDIOS}	SDIO to SCLK Rising Edge DATA Setup Time	400	-	-	ns
T_{SDIOH}	SCLK falling Edge to SDIO DATA Hold Time	0	-	600	ns

Table 10: Two-wire Control Timing Parameters

9.8 Audio Interface Timing:

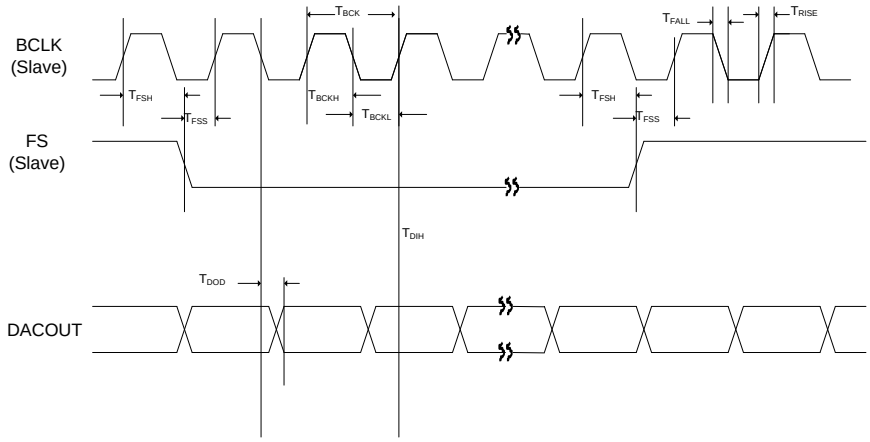


Figure 24: Digital Audio Interface Slave Mode Timing

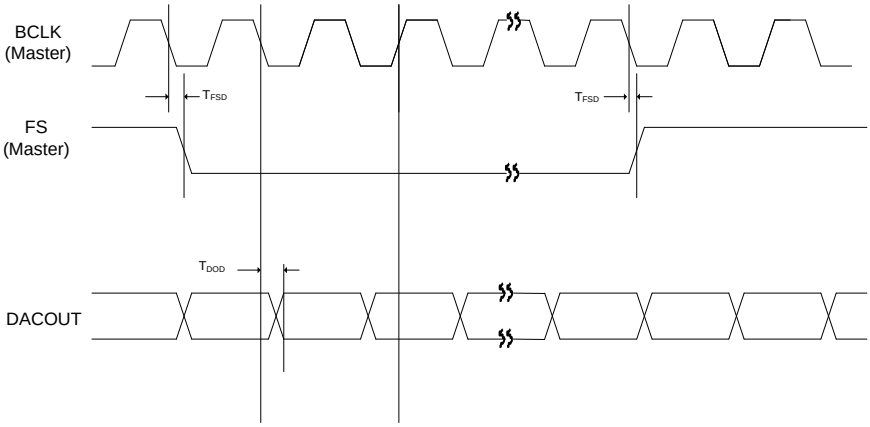


Figure 25: Digital Audio Interface Master Mode Timing

Symbol	Description	min	typ	max	unit
T_{BCK}	BCLK Cycle Time in Slave Mode	50	-	-	ns
T_{BCKH}	BCLK High Pulse Width in Slave Mode	20	-	-	ns
T_{BCKL}	BCLK Low Pulse Width in Slave Mode	20	-	-	ns
T_{FSS}	FS to BCLK Rising Edge Setup Time in Slave Mode	20	-	-	ns
T_{FSH}	BCLK Rising Edge to FS Hold Time in Slave Mode	20	-	-	ns
T_{FSD}	BCLK Falling Edge to FS Delay Time in Master Mode	-	-	10	ns
T_{RISE}	Rise Time for All Audio Interface Signals	-	-	$0.135T_{BCK}$	ns
T_{FALL}	Fall Time for All Audio Interface Signals	-	-	$0.135T_{BCK}$	ns
T_{DOD}	BCLK Falling Edge to DACOUT Delay Time	-	-	10	ns

Table 11: Audio Interface Timing Parameters

10 Application Information

10.1 Typical Application Schematic

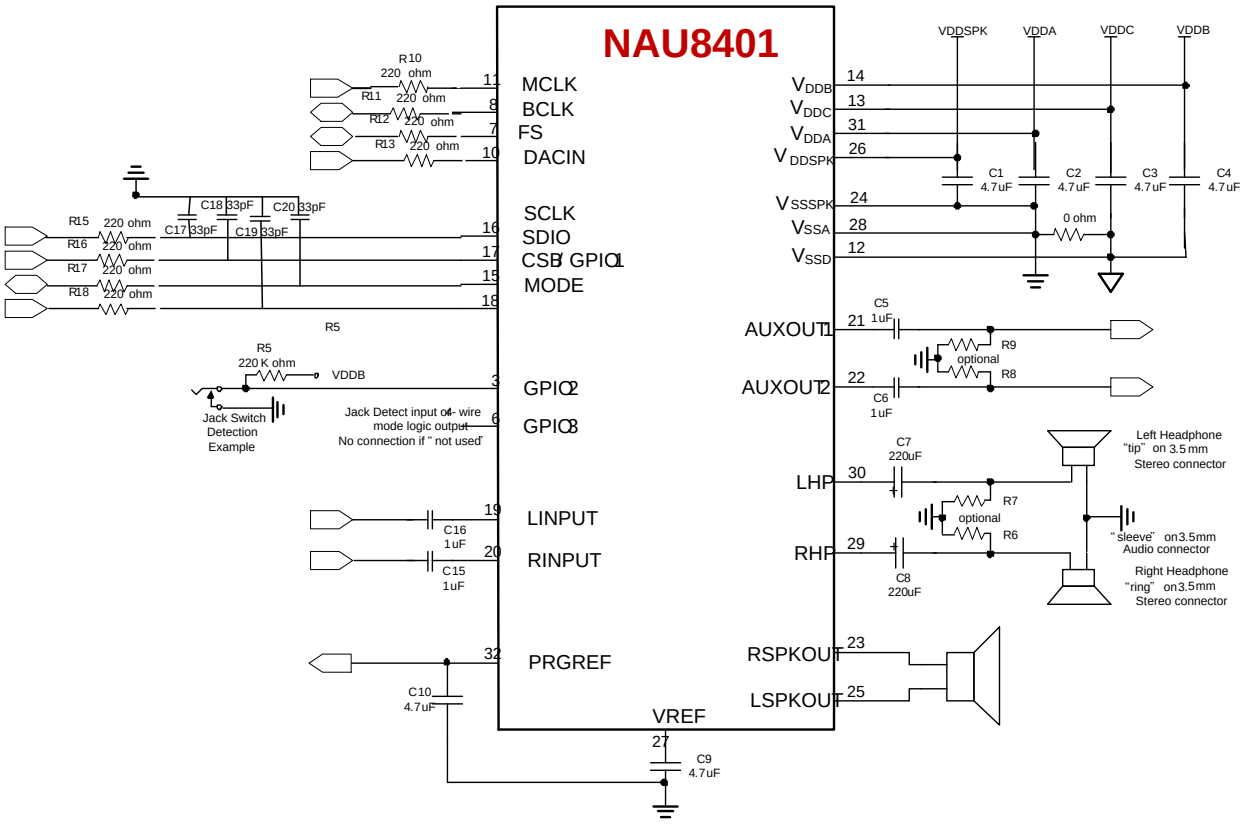


Figure 26: Schematic with recommended external components for typical application with AC-coupled headphones and stereo electret (ECM) style microphones.

Note 1: All non-polar capacitors are assumed to be low ESR type parts, such as with MLC construction or similar. If capacitors are not low ESR, additional 0.1ufd and/or 0.01ufd capacitors may be necessary in parallel with the bulk 4.7ufd capacitors on the supply rails.

Note 2: Load resistors to ground on outputs may be helpful in some applications to insure a DC path for the output capacitors to charge/discharge to the desired levels. If the output load is always present and the output load provides a suitable DC path to ground, then the additional load resistors may not be necessary. If needed, such load resistors are typically a high value, but a value dependent upon the application requirements.

Note 3: To minimize pops and clicks, large polarized output capacitors should be a low leakage type.

Note 4: Unused analog input pins should be left as no-connection.

Note 5: Unused digital input pins should be tied to ground.

Note 6: R15-R18 and C17-C20 for low pass filter to filter glitch; the corner frequency range of low pass filter is from 8MHz to 33MHz depending on PCB parasitic.

10.2 Recommended power up and power down sequences

To minimize pop and click noise, the NAU8401 should be powered up and down using the procedures in this section as guidance. The power-up procedure should be followed upon system power-up, or after any time that the NAU8401 has been issued a register reset command.

The strongest cause of pops and clicks in most system is the sudden charging or discharging of capacitors used for AC-coupling to inputs and outputs. Any sudden change in voltage will cause a pop or click, with or without AC-coupling capacitors in the signal path. The general strategy for pop and click reduction is to allow such charging and discharging to happen slowly.

10.2.1 Power Up (and after a software generated register reset) Procedure Guidance

Turn on external power supplies and wait for supply voltages to settle. This amount of time will be dependent on the system design. Software may choose to test the NAU8401 to determine when it is no longer in an active reset condition. This procedure is described in more detail in the sections relating to power supplies.

If the VDDSPK supply voltage is 3.60V or less, the next step should be to configure all of the output registers for low voltage operation. This sets the internal DC levels and gains to optimal levels for operation at lower voltages. Register settings required for this are:

R3 Bit 4, BIASGEN, set to logic = 1
R49 Bit 2, SPKBST; Bit 3, AUX2BST; Bit 4, AUX1BST, set to logic = 1

As a general policy, it is a good idea to put any input or output driver paths into the “mute” condition any time internal register and data path configurations are being changed. Be sure at this time that all used inputs and outputs are in their muted/disconnected condition.

Next, the internal DC tie-off voltage buffers should be enabled:

R1 Bit 2, IOBUFEN, set to logic = 1
R1 Bit 8, DCBUFEN, set to logic = 1 if setting up for greater than 3.60V operation

Value to be written to R1 = 0x104

At this point, the NAU8401 has been prepared to start charging any input/output capacitors to their normal operating mode charge state. If this is done slowly, then there will be no pops and clicks. One way to accomplish this is to allow the internal/external reference voltage to charge slowly by means of its internal coupling resistors. This is accomplished by:

R1 Bits 1, Bit 0, REFIMP set to 80kΩ setting
R1 Bit 2, ABIASEN, set to logic = 1
Value to be written to R1 = 0x10D

After this, the system should wait approximately 250ms, or longer, depending on the external components that have been selected for a given specific application.

After this, outputs may be enabled, but with the drivers still in the mute condition. Unless power management requires outputs to be turned off when not used, it is best for pops and clicks to leave outputs enabled at all times, and to use the output mute controls to silence the outputs as needed.

Next, the NAU8401 can be programmed as needed for a specific application. The final step in most applications will be to unmute any outputs, and then begin normal operation.

10.2.2 Power Down

Powering down is more application specific. The most important step is to mute all outputs before any other steps. It then may be further helpful to disable all outputs just before the system power-down sequence is started.

10.2.3 Unused Input/Output Tie-Off Information

In audio and voice systems, any time there is a sudden change in voltage to an audio signal, an audible pop or click sound may be the result. Systems that change inputs and output configurations dynamically, or which are required to manage low power operation, need special attention to possible pop and click situations.

The NAU8401 includes many features which may be used to greatly reduce or eliminate pop and click sounds. The most common cause of a pop or click signal is a sudden change to an input or output voltage. This may happen in either a DC coupled system, or in an AC coupled system.

The strategy to control pops and clicks is similar for either a DC coupled system, or an AC coupled system. The case of the AC coupled system is the most common and the more difficult situation, and therefore, the AC coupled case will the focus for this information section.

When an input or output pin is being used, the DC level of that pin will be very close to ½ of the VDDA voltage that is present on the VREF pin. The only exception is that when outputs are operated in the 5-Volt mode known as the 1.5X boost condition, then the DC level for those outputs will be equal to 1.5xVREF.

In all cases, any input or output capacitors will become charged to the operating voltage of the used input or output pin. The goal to reduce pops and clicks is to insure that the charge voltage on these capacitors does not change suddenly at any time.

When an input or output is in a not-used operating condition, it is desirable to keep the DC voltage on that pin at the same voltage level as the DC level of the used operating condition. This is accomplished using special internal DC voltage sources that are at the required DC values. When an input or output is in the not-used condition, it is connected to the correct internal DC voltage as not to have a pop or click. This type of connection is known as a "tie-off" condition.

Two internal DC voltage sources are provided for making tie-off connections. One DC level is equal to the VREF voltage value, and the other DC level is equal to 1.5X the VREF value. All inputs are always tied off to the VREF voltage value. Outputs will automatically be tied to either the VREF voltage value or to the 1.5xVREF value, depending on the value of the "boost" control bit for that output. That is to say, when an output is set to the 1.5X gain condition, then that same output will automatically use the 1.5xVREF value for tie-off in the not-used condition.

To conserve power, these internal voltage buffers may be enabled/disabled using control register settings. To better manage pops and clicks, there is a choice of impedance of the tie-off connection for unused outputs. The nominal values for this choice are 1kΩ and 30kΩ. The low impedance value will better maintain the desired DC level in the case when there is some leakage on the output capacitor or some DC resistance to ground at the NAU8401 output pin. A tradeoff in using the low-impedance value is primarily that output capacitors could change more suddenly during power-on and power-off changes.

Automatic internal logic determines whether an input or output pin is in the used or un-used condition. This logic function is always active. An output is determined to be in the un-used condition when it is in the disabled unpowered condition, as determined by the power management registers. An input is determined to be in the un-used condition when all internal switches connected to that input are in the "open" condition.

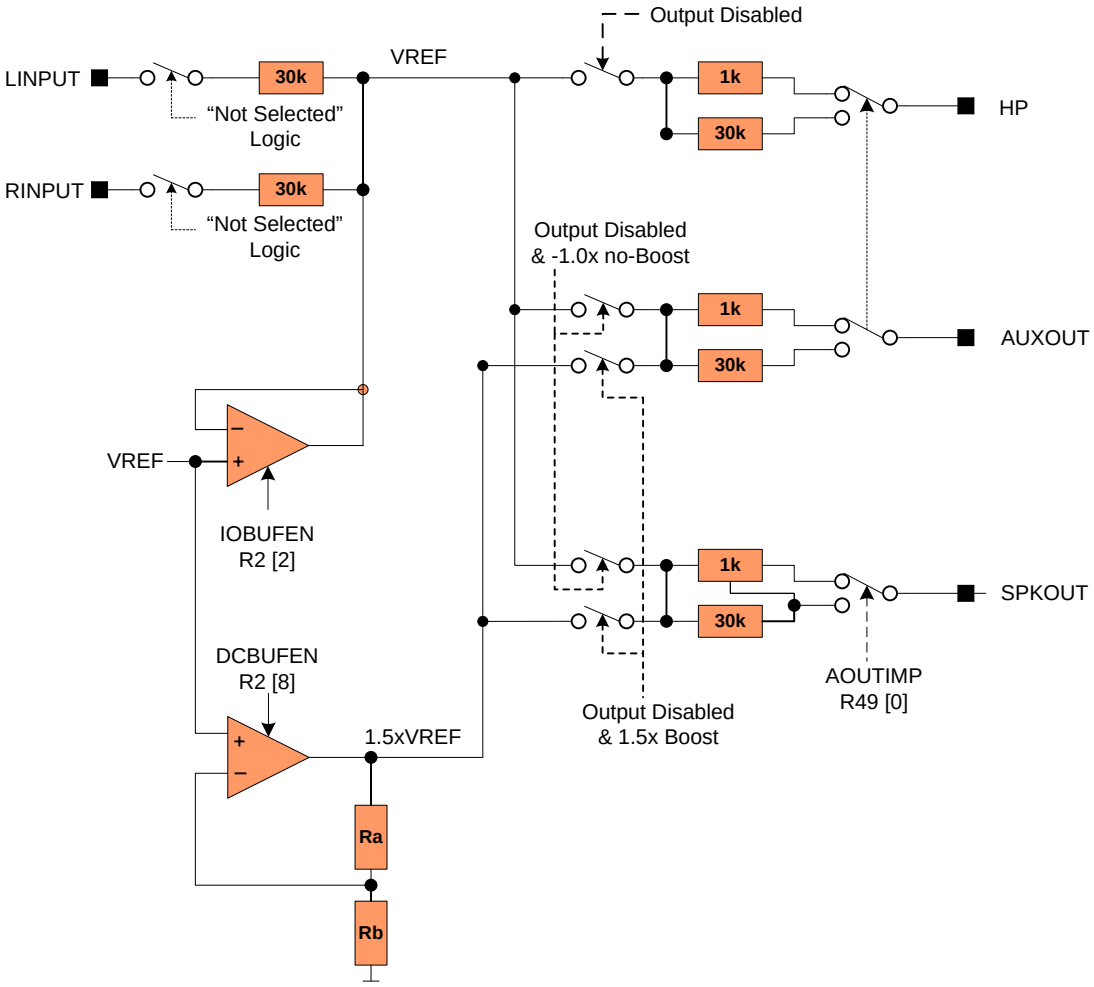


Figure 27: Tie-off Options for input and output pin examples

Register settings that directly affect the tie-off features are:

Register 1, Bit 2 Enable buffer for VREF tie-off (value = 1 = enabled)
Register 1, Bit 8 Enable buffer for 1.5xVREF tie-off (value = 1 = enabled)
Register 49, Bit 0 Tie-off impedance selection (0 = 1kΩ, 1 = 30kΩ)

Note: Resistor tie-off switches will open/close regardless of whether or not the associated internal DC buffer is in the enabled or disabled condition.

10.3 Power Consumption

The NAU8401 has flexible power management capability which allows sections not being used to be powered down, to draw minimum current in battery-powered applications. The following table shows typical power consumption in different operating conditions. The "off" condition is the initial power-on state with all subsystems powered down, and with no applied clocks.

Mode	Conditions	VDDA = 3V	VDDC = 1.8V	VDDB = 3V	Total Power
		mA	mA	mA	mW
OFF		0.008	0.001	0.0003	0.025
Sleep	VREF maintained @ 300kΩ, no clocks,	0.009	0.001	0.0003	0.028
	VREF maintained @ 75kΩ, no clocks,	0.014	0.001	0.0003	0.045
	VREF maintained @ 5kΩ, no clocks,	0.259	0.001	0.0003	0.781
Stereo Playback	16Ω HP, 44.1kHz, quiescent	7.25	6.10	0.03	32.8
	16Ω HP, 44.1kHz, quiescent, PLL on	9.77	7.53	0.025	42.9
	16Ω HP, 44.1kHz, 0.6 Vrms sine wave	21.3	6.28	0.015	75.2
	16Ω HP, 44.1kHz, 0.6Vrms sine, PLL on	23.8	7.72	0.015	85.3

Table 12: Typical Power Consumption in Various Application Modes.

10.4 Supply Currents of Specific Blocks

The NAU8401 can be programmed to enable/disable various analog blocks individually, and the current to some of the major blocks can be reduced with minimum impact on performance. The table below shows the change in current consumed with different register settings. Sample rate settings affect current consumption of VDDC supply. Lower sampling rates draw lower current.

Register		Function	Bit	VDDA current increase/ Decrease when enabled
Dec	Hex			
1	01	Power Management 1	REFIMP[1:0]	+100µA for 80kΩ and 300kΩ +260µA for 3kΩ
			IOBUFEN[2]	+100µA
			ABIASEN[3]	+600µA
			PRGREFEN[4]	+540µA
			PLLEN[5]	+2.5 mA +1/5mA from VDDC with clocks applied
			AUX2MXEN[6]	+200µA
			AUX1MXEN[7]	+200µA
			DCBUFEN[8]	+140µA
1	01	Power Management 2	SLEEP[6]	Same as PLLEN (R1[5])
			LHPEN[7]	+800µA
			RHPEN[8]	+800µA
3	03	Power Management 3	LMIXEN[2]	+250µA
			RMIXEN[3]	+250µA
			BIASGEN[4]	+150uA
			RSPKEN[5]	+1.1 mA from VDDSPK
			LSPKEN[6]	+1.1 mA from VDDSPK
			AUXOUT2EN[7] AUXOUT1EN[8]	+225µA +225µA
58	3A	Power Management 4	IBIADJ[1:0]	-1.2mA with IBIADJ at 11
			REGVOLT[2:3]	
			PRGREFM[4]	
			LPSPKD[5]	
			LPDAC[8]	-1.1mA with 1.4dB SNR decrease @ 44.1kHz

Table 13: VDDA 3.3V Supply Current in Various Modes

11 Appendix A: Digital Filter Characteristics

Parameter	Conditions	Min	Typ	Max	Units
Passband	+/- 0.035dB	0		0.454	fs
	-6dB		0.5		fs
Passband Ripple				+/-0.035	dB
Stopband		0.546			fs
Stopband Attenuation	f > 0.546*fs	-55			dB
Group Delay			28		1/fs

Table 14: DAC Digital Filter Characteristics

TERMINOLOGY

1. Stop Band Attenuation (dB) – the degree to which the frequency spectrum is attenuated (outside audio band)
2. Pass-band Ripple – any variation of the frequency response in the pass-band region
3. Note that this delay applies only to the filters and does not include other latencies, such as from the serial data interface

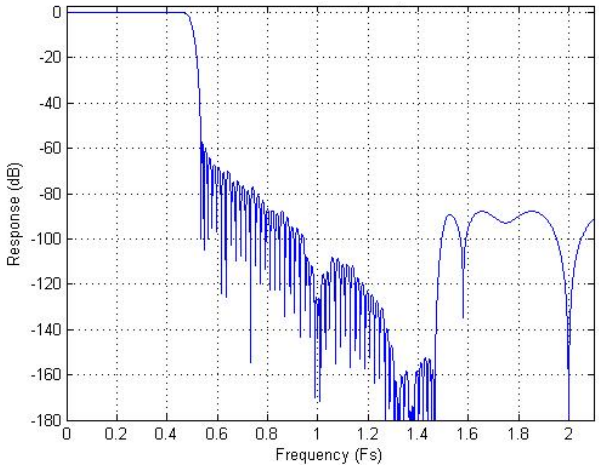


Figure 28: DAC Filter Frequency Response

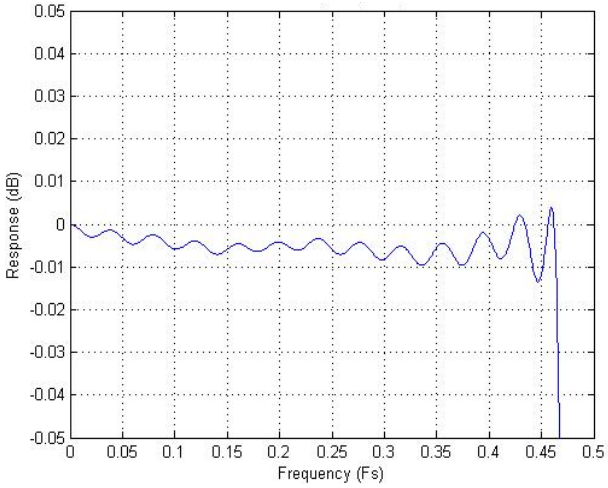


Figure 29: DAC Filter Ripple

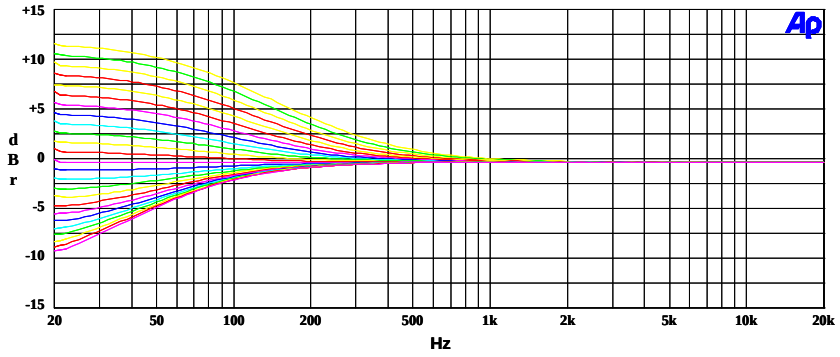


Figure 30: EQ Band 1 Gains for Lowest Cut-Off Frequency

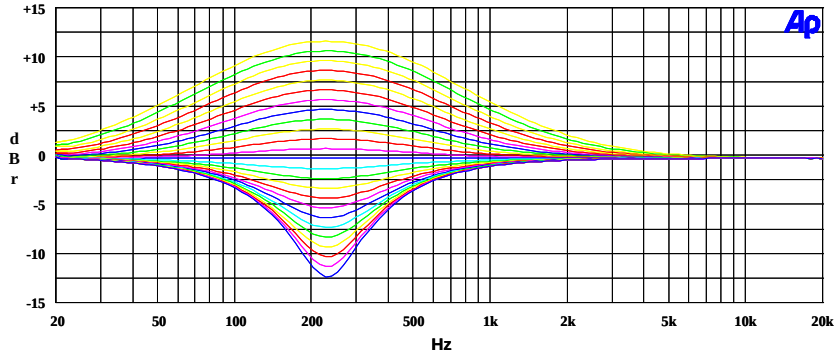


Figure 31: EQ Band 2 Peak Filter Gains for Lowest Cut-Off Frequency with EQ2BW = 0

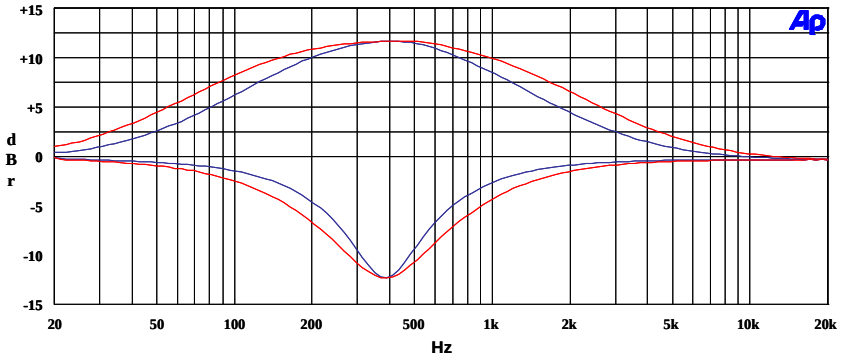


Figure 32: EQ Band 2, EQ2BW = 0 versus EQ2BW = 1

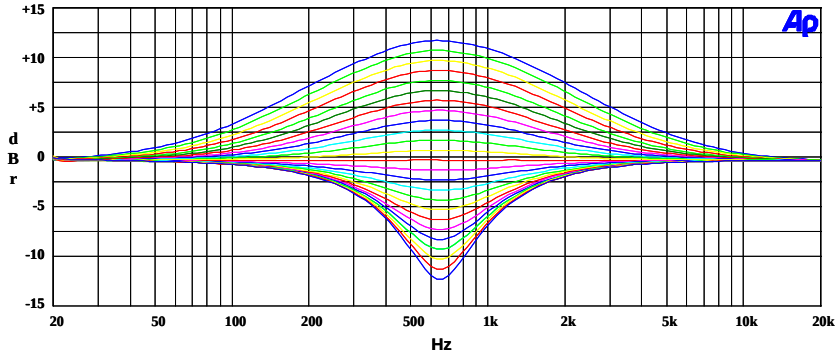


Figure 33: EQ Band 3 Peak Filter Gains for Lowest Cut-Off Frequency with EQ3BW = 0

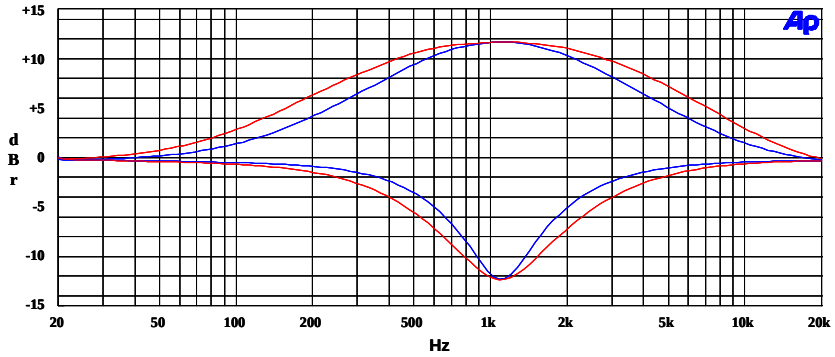


Figure 34: EQ Band 3, EQ3BW = 0 versus EQ3BW = 1

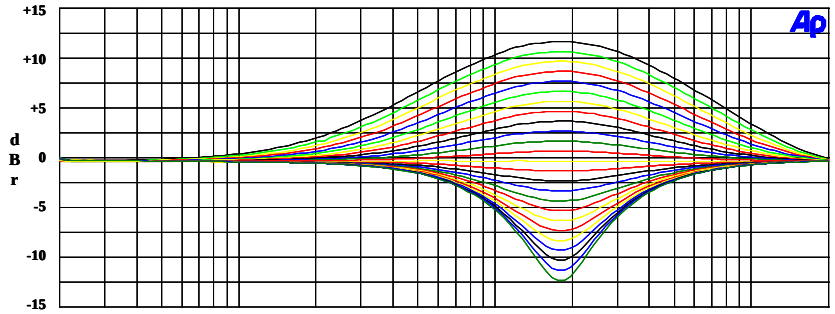


Figure 35: EQ Band 4 Peak Filter Gains for Lowest Cut-Off Frequencies with EQ4BW = 0

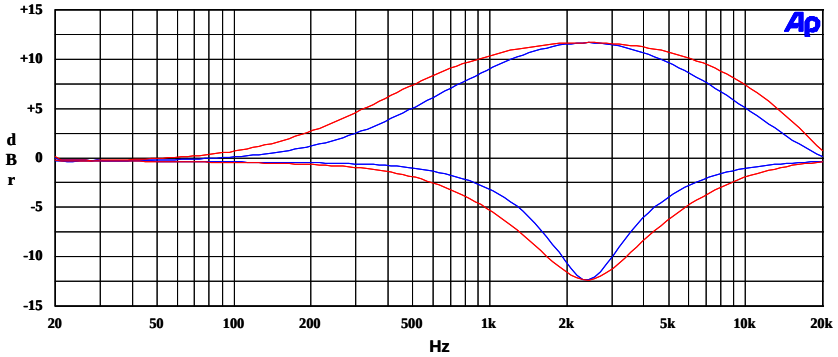


Figure 36: EQ Band 4, EQ4BW = 0 versus EQ4BW =1

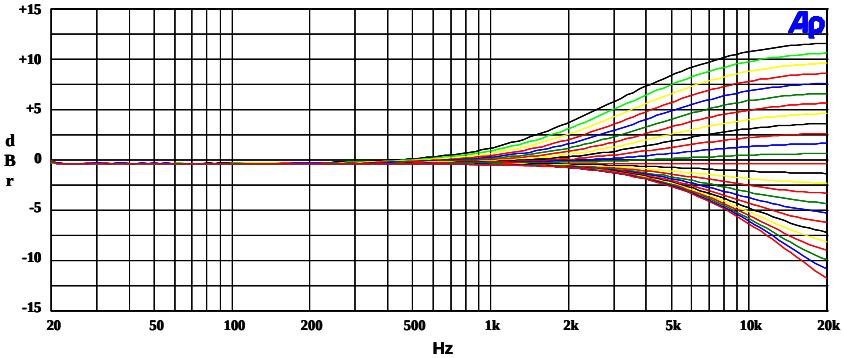


Figure 37: EQ Band 5 Gains for Lowest Cut-Off Frequency

12 Appendix B: Companding Tables

12.1 µ-Law / A-Law Codes for Zero and Full Scale

Level	µ-Law			A-Law		
	Sign bit (D7)	Chord bits (D6,D5,D4)	Step bits (D3,D2,D1,D0)	Sign bit (D7)	Chord bits (D6,D5,D4)	Step bits (D3,D2,D1,D0)
+ Full Scale	1	000	0000	1	010	1010
+ Zero	1	111	1111	1	101	0101
- Zero	0	111	1111	0	101	0101
- Full Scale	0	000	0000	0	010	1010

Table 15: Companding Codes for Zero and Full-Scale

12.2 µ-Law / A-Law Output Codes (Digital mW)

Sample	µ-Law			A-Law		
	Sign bit (D7)	Chord bits (D6,D5,D4)	Step bits (D3,D2,D1,D0)	Sign bit (D7)	Chord bits (D6,D5,D4)	Step bits (D3,D2,D1,D0)
1	0	001	1110	0	011	0100
2	0	000	1011	0	010	0001
3	0	000	1011	0	010	0001
4	0	001	1110	0	011	0100
5	1	001	1110	1	011	0100
6	1	000	1011	1	010	0001
7	1	000	1011	1	010	0001
8	1	001	1110	1	011	0100

Table 16: Companding Output Codes

13 Appendix C: Details of Register Operation

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
0	00	Software Reset											Any write operation to this register resets all registers to default values
1	01	Power Management 1	DCBUFEN										Power control for internal tie-off buffer used in 1.5X boost conditions 0 = internal buffer unpowered 1 = enabled
			AUX1MXEN										Power control for AUX1 MIXER supporting AUXOUT1 analog output 0 = unpowered 1 = enabled
			AUX2MXEN										Power control for AUX2 MIXER supporting AUXOUT2 analog output 0 = unpowered 1 = enabled
			PLLEN										Power control for internal PLL 0 = unpowered 1 = enabled
			PRGREF										Power control for refernce voltage bias buffer amplifier (PRGREF output, pin#32) 0 = unpowered and PRGREF pin in high-Z condition 1 = enabled
			ABIASEN										Power control for internal analog bias buffers 0 = unpowered 1 = enabled
			IOBUFEN										Power control for internal tie-off buffer used in non-boost mode (-1.0x gain) conditions 0 = internal buffer unpowered 1 = enabled
			REFIMP										Select impedance of reference string used to establish VREF for internal bias buffers 00 = off (input to internal bias buffer in high-Z floating condition) 01 = 80kΩ nominal impedance at VREF pin 10 = 300kΩ nominal impedance at VREF pin 11 = 3kΩ nominal impedance at VREF pin
			Default >>	0	0	0	0	0	0	0	0	0	0x000 reset value
2	02	Power Management 2	RHPEN										Right Headphone driver enable, RHP analog output, pin#29 0 = RHP pin in high-Z condition 1 = enabled
			LHPEN										Left Headphone driver enabled, LHP analog output pin#30 0 = LHP pin in high-Z condition 1 = enabled
			SLEEP										Sleep enable 0 = device in normal operating mode 1 = device in low-power sleep condition
			Reserved										Reserved
			Default >>	0	0	0	0	0	0	0	0	0	0x000 reset value

Register		Function	Name	Bit									Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
3	03	Power Management 3	AUXOUT1EN										AUXOUT1 analog output power control, pin#21 0 = AUXOUT1 output driver OFF 1 = enabled
			AUXOUT2EN										AUXOUT2 analog output power control, pin#22 0 = AUXOUT2 output driver OFF 1 = enabled
			LSPKEN										LSPKOUT left speaker driver power control, pin#25 0 = LSPKOUT output driver OFF 1 = enabled
			RSPKEN										RSPKOUT left speaker driver power control, pin#23 0 = RSPKOUT output driver OFF 1 = enabled
			BIASGEN										Bias control for high current output when outputs are in 1.5X boost mode 0 = reduced current operation and reduced max output current 1 = normal operation enabling outputs to deliver full rated output current
			RMIXEN										Right main mixer power control, RMAIN MIXER internal stage 0 = RMAIN MIXER stage OFF 1 = enabled
			LMIXEN										Left main mixer power control, LMAIN MIXER internal stage 0 = LMAIN MIXER stage OFF 1 = enabled
			RDACEN										Right channel digital-to-analog converter, RDAC, power control 0 = RDAC stage OFF 1 = enabled
			LDACEN										Left channel digital-to-analog converter, LDAC, power control 0 = LDAC stage OFF 1 = enabled
			Default >>	0	0	0	0	0	0	0	0	0	0x000 reset value
4	04	Audio Interface	BCLKP										Bit clock phase inversion option for BCLK, pin#8 0 = normal phase 1 = input logic sense inverted
			LRP										Phase control for I2S audio data bus interface 0 = normal phase operation 1 = inverted phase operation PCMA and PCMB left/right word order control 0 = MSB is valid on 2nd rising edge of BCLK after rising edge of FS 1 = MSB is valid on 1st rising edge of BCLK after rising edge of FS
			WLEN										Word length (24-bits default) of audio data stream 00 = 16-bit word length 01 = 20-bit word length 10 = 24-bit word length 11 = 32-bit word length
			AIFMT										Audio interface data format (default setting is I2S) 00 = right justified 01 = left justified 10 = standard I2S format 11 = PCMA or PCMB audio data format option
			DACPHS										DAC audio data left-right ordering 0 = left DAC data in left phase of LRP 1 = left DAC data in right phase of LRP (left-right reversed)
			Reserved										Reserved
			MONO										Mono operation enable 0 = normal stereo mode of operation (default) 1 = mono mode with audio data in left phase of LRP
			Default >>	0	0	1	0	1	0	0	0	0	0x050 reset value

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
5	05	Companding	Reserved										Reserved
			CMB8										8-bit word enable for companding mode of operation 0 = normal operation (no companding) 1 = 8-bit operation for companding mode
			DACCM										DAC companding mode control 00 = off (normal linear operation) 01 = reserved 10 = u-law companding 11 = A-law companding
			Reserved										Reserved
			Default >>	0	0	0	0	0	0	0	0	0	0x000 reset value
6	06	Clock control 1	CLKM										master clock source selection control 0 = MCLK, pin#11 used as master clock 1 = internal PLL oscillator output used as master clock
			MCLKSEL										Scaling of master clock source for internal 256fs rate (divide by 2 = default) 000 = divide by 1 001 = divide by 1.5 010 = divide by 2 011 = divide by 3 100 = divide by 4 101 = divide by 6 110 = divide by 8 111 = divide by 12
			BCLKSEL										Scaling of output frequency at BCLK pin#8 when chip is in master mode 000 = divide by 1 001 = divide by 2 010 = divide by 4 011 = divide by 8 100 = divide by 16 101 = divide by 32 110 = reserved 111 = reserved
			Reserved										Reserved
			CLKIOEN										Enables chip master mode to drive FS and BCLK outputs 0 = FS and BCLK are inputs 1 = FS and BCLK are driven as outputs by internally generated clocks
			Default >>	1	0	1	0	0	0	0	0	0	0x140 reset value
7	07	Clock control 2	4WSPIEN										4-wire control interface enable
			Reserved										Reserved
			SMPLR										Audio data sample rate indication (48kHz default). Sets up scaling for internal filter coefficients, but does not affect in any way the actual device sample rate. Should be set to value most closely matching the actual sample rate determined by 256fs internal node. 000 = 48kHz 001 = 32kHz 010 = 24kHz 011 = 16kHz 100 = 12kHz 101 = 8kHz 110 = reserved 111 = reserved
			SCLKEN										Slow timer clock enable. Starts internal timer clock derived by dividing master clock. 0 = disabled 1 = enabled
			Default >>	0	0	0	0	0	0	0	0	0	0x000 reset value

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
8	08	GPIO	Reserved										Reserved
			GPIO1PLL										Clock divisor applied to PLL clock for output from a GPIO pin 00 = divide by 1 01 = divide by 2 10 = divide by 3 11 = divide by 4
			GPIO1PL										GPIO1 polarity inversion control 0 = normal logic sense of GPIO signal 1 = inverted logic sense of GPIO signal
			GPIO1SEL										CSB/GPIO1 function select (input default) 000 = use as input subject to MODE pin#18 input logic level 001 = reserved 010 = Temperature OK status output (logic 0 = thermal shutdown) 011 = DAC automute condition (logic 1 = one or both DACs automuted) 100 = output divided PLL clock 101 = PLL locked condition (logic 1 = PLL locked) 110 = output set to logic 1 condition 111 = output set to logic 0 condition
			Default >>	0	0	0	0	0	0	0	0	0	0x000 reset value
9	09	Jack detect 1	JCKMIDEN										Automatically enable internal bias amplifiers on jack detection state as sensed through GPIO pin associated to jack detection function Bit 7 = logic 1: enable bias amplifiers on jack at logic 0 level Bit 8 = logic 1: enable bias amplifiers on jack at logic 1 level
			JACDEN										Jack detection feature enable 0 = disabled 1 = enable jack detection associated functionality
			JCKDIO										Select jack detect pin (GPIO1 default) 00 = GPIO1 is used for jack detection feature 01 = GPIO2 is used for jack detection feature 10 = GPIO3 is used for jack detection feature 11 = reserved
			Reserved										Reserved
			Default >>	0	0	0	0	0	0	0	0	0	0x000 reset value
10	0A	DAC control	Reserved										Reserved
			SOFTMT										Softmute feature control for DACs 0 = disabled 1 = enabled
			Reserved										Reserved
			DACOS										DAC oversampling rate selection (64X default) 0 = 64x oversampling 1 = 128x oversampling
			AUTOMT										DAC automute function enable 0 = disabled 1 = enabled
			RDACPL										DAC right channel output polarity control 0 = normal polarity 1 = inverted polarity
			LDACPL										DAC left channel output polarity control 0 = normal polarity 1 = inverted polarity
			Default >>	0	0	0	0	0	0	0	0	0	0x000 reset value
11	0B	Left DAC volume	LDACVU										DAC volume update bit feature. Write-only bit for synchronized L/R DAC changes If logic = 0 on R11 write, new R11 value stored in temporary register If logic = 1 on R11 write, new R11 and pending R12 values become active
			LDACGAIN										DAC left digital volume control (0dB default attenuation value). Expressed as an attenuation value in 0.5dB steps as follows: 0000 0000 = digital mute condition 0000 0001 = -127.0dB (highly attenuated) 0000 0010 = -126.5dB attenuation - all intermediate 0.5 step values through maximum – 1111 1110 = -0.5dB attenuation 1111 1111 = 0.0dB attenuation (no attenuation)
			Default >>	0	1	1	1	1	1	1	1	1	0x0FF reset value

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
12	0C	Right DAC volume	RDACVU										DAC volume update bit feature. Write-only bit for synchronized L/R DAC changes If logic = 0 on R12 write, new R12 value stored in temporary register If logic = 1 on R12 write, new R12 and pending R11 values become active
			RDACGAIN										DAC right digital volume control (0dB default attenuation value). Expressed as an attenuation value in 0.5dB steps as follows: 0000 0000 = digital mute condition 0000 0001 = -127.0dB (highly attenuated) 0000 0010 = -126.5dB attenuation - all intermediate 0.5 step values through maximum volume – 1111 1110 = -0.5dB attenuation 1111 1111 = 0.0dB attenuation (no attenuation)
			Default >>	0	1	1	1	1	1	1	1	1	0x0FF reset value
13	0D	Jack detect 2	Reserved										Reserved
			JCKDOEN1										Outputs drivers that are automatically enabled whenever the designated jack detection input is in the logic = 1 condition, and the jack detection feature is enabled Bit 4 = 1: enable Left and Right Headphone output drivers Bit 5 = 1: enable Left and Right Speaker output drivers Bit 6 = 1: enable AUXOUT2 output driver Bit 7 = 1: enable AUXOUT1 output driver
			JCKDOEN0										Outputs drivers that are automatically enabled whenever the designated jack detection input is in the logic = 0 condition, and the jack detection feature is enabled Bit 0 = 1: enable Left and Right Headphone output drivers Bit 1 = 1: enable Left and Right Speaker output drivers Bit 2 = 1: enable AUXOUT2 output driver Bit 3 = 1: enable AUXOUT1 output driver
			Default >>	0	0	0	0	0	0	0	0	0	0x000 reset value
14	0E	Reserved	Reserved										Reserved
15	0F	Reserved	Reserved										Reserved
16	10	Reserved	Reserved										Reserved
17	11	Reserved	Reserved										Reserved
18	12	EQ1 low cutoff	EQM										Equalizer and 3D audio processing block assignment. 0 = block disabled on digital stream from DAC 1 = block operates on digital stream to DAC (default on reset)
			Reserved										Reserved
			EQ1CF										Equalizer band 1 low pass -3dB cut-off frequency selection 00 = 80Hz 01 = 105Hz (default) 10 = 135Hz 11 = 175Hz
			EQ1GC										EQ Band 1 digital gain control. Expressed as a gain or attenuation in 1dB steps 01100 = 0.0dB default unity gain value 00000 = +12dB 00001 = +11dB - all intermediate 1.0dB step values through minimum gain - 11000 = -12dB 11001 and larger values are reserved
			Default >>	1	0	0	1	0	1	1	0	0	0x12C reset value

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
19	13	EQ2 - peak 1	EQ2BW										Equalizer Band 2 bandwidth selection 0 = narrow band characteristic (default) 1 = wide band characteristic
			Reserved										Reserved
			EQ2CF										Equalizer Band 2 center frequency selection 00 = 230Hz 01 = 300Hz (default) 10 = 385Hz 11 = 500Hz
			EQ2GC										EQ Band 2 digital gain control. Expressed as a gain or attenuation in 1dB steps 01100 = 0.0dB default unity gain value 00000 = +12dB 00001 = +11dB - all intermediate 1.0dB step values through minimum gain - 11000 = -12dB 11001 and larger values are reserved
			Default >>	0	0	0	1	0	1	1	0	0	0x02C reset value
20	14	EQ3 - peak 2	EQ3BW										Equalizer Band 3 bandwidth selection 0 = narrow band characteristic (default) 1 = wide band characteristic
			Reserved										Reserved
			EQ3CF										Equalizer Band 3 center frequency selection 00 = 650Hz 01 = 850Hz (default) 10 = 1.1kHz 11 = 1.4kHz
			EQ3GC										EQ Band 3 digital gain control. Expressed as a gain or attenuation in 1dB steps 01100 = 0.0dB default unity gain value 00000 = +12dB 00001 = +11dB - all intermediate 1.0dB step values through minimum gain - 11000 = -12dB 11001 and larger values are reserved
			Default >>	0	0	0	1	0	1	1	0	0	0x02C reset value
21	15	EQ4 - peak 3	EQ4BW										Equalizer Band 4 bandwidth selection 0 = narrow band characteristic (default) 1 = wide band characteristic
			Reserved										Reserved
			EQ4CF										Equalizer Band 4 center frequency selection 00 = 1.8kHz 01 = 2.4kHz (default) 10 = 3.2kHz 11 = 4.1kHz
			EQ4GC										EQ Band 4 digital gain control. Expressed as a gain or attenuation in 1dB steps 01100 = 0.0dB default unity gain value 00000 = +12dB 00001 = +11dB - all intermediate 1.0dB step values through minimum gain - 11000 = -12dB 11001 and larger values are reserved
			Default >>	0	0	0	1	0	1	1	0	0	0x02C reset value

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
22	16	EQ5 - high cutoff	Reserved										Reserved
			EQ5CF										Equalizer Band 5 high pass -3dB cut-off frequency selection 00 = 5.3kHz 01 = 6.9kHz (default) 10 = 9.0kHz 11 = 11.7kHz
			EQ5GC										EQ Band 5 digital gain control. Expressed as a gain or attenuation in 1dB steps 01100 = 0.0dB default unity gain value 00000 = +12dB 00001 = +11dB - all intermediate 1.0dB step values through minimum gain - 11000 = -12dB 11001 and larger values are reserved
			Default >>	0	0	0	1	0	1	1	0	0	0x02C reset value
23	17	Reserved	Reserved										Reserved
24	18	DAC limiter 1	DACLIMEN										DAC digital limiter control bit 0 = disabled 1 = enabled
			DACLIMDCY										DAC limiter decay time. Proportional to actual DAC sample rate. Duration doubles with each binary bit value. Values given here are for 44.1kHz sample rate 0000 = 0.544ms 0001 = 1.09ms 0010 = 2.18ms 0011 = 4.36ms (default) 0100 = 8.72ms 0101 = 17.4ms 0110 = 34.8ms 0111 = 69.6ms 1000 = 139ms 1001 = 278ms 1010 = 566ms 1011 through 1111 = 1130ms
			DACLIMATK										DAC limiter attack time. Proportional to actual DAC sample rate. Duration doubles with each binary bit value. Values given here are for 44.1kHz sample rate 0000 = 68.0us (microseconds) 0001 = 136us 0010 = 272us (default) 0011 = 544us 0100 = 1.09ms (milliseconds) 0101 = 2.18ms 0110 = 4.36ms 0111 = 8.72ms 1000 = 17.4ms 1001 = 34.8ms 1010 = 69.6ms 1011 through 1111 = 139ms
			Default >>	0	0	0	1	1	0	0	1	0	0x032 reset value
25	19	DAC limiter 2	Reserved										Reserved
			DACLIMTHL										DAC limiter threshold in relation to full scale output level (0.0dB = full scale) 000 = -1.0dB 001 = -2.0dB 010 = -3.0dB 011 = -4.0dB 100 = -5.0dB 101 through 111 = -6.0dB
			DACLIMBST										DAC limiter maximum automatic gain boost in limiter mode. If R24 limiter mode is disabled, specified gain value will be applied in addition to other gain values in the signal path. 0000 = 0.0dB (default) 0001 = +1.0dB - Gain value increases in 1.0dB steps for each binary value – 1100 = +12dB (maximum allowed boost value) 1101 through 1111 = reserved
			Default >>	0	0	0	0	0	0	0	0	0	0x000 reset value
26	1A	Reserved	Reserved										Reserved

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
27	1B	Reserved	Reserved										Reserved
28	1C	Reserved	Reserved										Reserved
29	1D	Reserved	Reserved										Reserved
30	1E	Reserved	Reserved										Reserved
31	1F	Reserved	Reserved										Reserved
32	20	Reserved	Reserved										Reserved
33	21	Reserved	Reserved										Reserved
34	22	Reserved	Reserved										Reserved
35	23	Reserved	Reserved										Reserved
36	24	PLL N	Reserved										Reserved
			PLLMCLK										Control bit for divide by 2 pre-scale of MCLK path to PLL clock input 0 = MCLK divide by 1 (default) 1 = MCLK divide by 2
			PLLN										Integer portion of PLL input/output frequency ratio divider. Decimal value should be constrained to 6, 7, 8, 9, 10, 11, or 12. Default decimal value is 8. See text for details.
			Default >>	0	0	0	0	0	1	0	0	0	0x008 reset value
37	25	PLL K 1	Reserved										Reserved
			PLLK[23:18]										High order bits of fractional portion of PLL input/output frequency ratio divider. See text for details.
			Default >>	0	0	0	0	0	1	1	0	0	0x00C reset value
38	26	PLL K 2	PLLK[17:9]										Middle order bits of fractional portion of PLL input/output frequency ratio divider. See text for details.
			Default >>	0	1	0	0	1	0	0	1	1	0x093 reset value
39	27	PLL K 3	PLLK{8:0]										Low order bits of fractional portion of PLL input/output frequency ratio divider. See text for details.
			Default >>	0	1	1	1	0	1	0	0	1	0x0E9 reset value
40	28	PRGREF Mode	Reserved										Reserved
			PRGREFM										Programmable reference optional low noise mode configuration control 0 = normal configuration with low-Z PRGREF output impedance 1 = low noise configuration with 200-ohm PRGREF output impedance
			Default >>	0	0	0	0	0	0	0	0	0	0x000 reset value
41	29	3D control	Reserved										Reserved
			3DDEPTH										3D Stereo Enhancement effect depth control 0000 = 0.0% effect (disabled, default) 0001 = 6.67% effect 0010 = 13.3% effect - effect depth varies by 6.67% per binary bit value – 1110 = 93.3% effect 1111 = 100% effect (maximum effect)
			Default >>	0	0	0	0	0	0	0	0	0	0x000 reset value
42	2A	Reserved	Reserved										
43	2B		Reserved										Reserved

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
		Right Speaker Submixer	RMIXMUT										Mutes the RMIX speaker signal gain stage output in the right speaker submixer 0 = gain stage output enabled 1 = gain stage output muted
			RSUBBYP										Right speaker submixer bypass control 0 = right speaker amplifier directly connected to RMIX speaker signal gain stage 1 = right speaker amplifier connected to submixer output (inverts RMIX for BTL)
			RAUXRSUBG										RINPUT to Right Speaker Submixer input gain control 000 = -15dB (default) 001 = -12dB 010 = -9.0dB 011 = -6.0dB 100 = -3.0dB 101 = 0.0dB 110 = +3.0dB 111 = +6.0dB
			RAUXSMUT										RINPUT to Right Speaker Submixer mute control 0 = RINPUT path to submixer is muted 1 = RINPUT path to submixer is enabled
			Default >>	0	0	0	0	0	0	0	0	0	0x000 reset value
44	2C	Input control	PRGREFV										Programmable reference voltage selection control. Values change slightly with R40 PRGREF mode selection control. Open circuit voltage on PRGREF pin#32 is shown as follows as a fraction of the VDDA pin#31 supply voltage. Normal Mode Low Noise Mode 00 = 0.9x 00 = 0.85x 01 = 0.65x 01 = 0.60x 10 = 0.75x 10 = 0.70x 11 = 0.50x 11 = 0.50x
			Reserved										Reserved
			Default >>	0	0	0	1	1	0	0	1	1	0x033 reset value
45	2D	Reserved	Reserved										Reserved
46	2E	Reserved	Reserved										Reserved
47	2F	Reserved	Reserved										Reserved
48	30	Reserved	Reserved										Reserved
49	31	Output control	Reserved										Reserved
			LDACRMX										Left DAC output to RMIX right output mixer cross-coupling path control 0 = path disconnected (default) 1 = path connected
			RDACLMX										Right DAC output to LMIX left output mixer cross-coupling path control 0 = path disconnected (default) 1 = path connected
			AUX1BST										AUXOUT1 gain boost control 0 = required setting for greater than 3.6V operation, +1.5x gain (default) 1 = preferred setting for 3.6V and lower operation, -1.0x gain
			AUX2BST										AUXOUT2 gain boost control 0 = required setting for greater than 3.6V operation, +1.5x gain (default) 1 = preferred setting for 3.6V and lower operation, -1.0x gain
			SPKBST										LSPKOUT and RSPKOUT speaker amplifier gain boost control 0 = required setting for greater than 3.6V operation, +1.5x gain (default) 1 = preferred setting for 3.6V and lower operation, -1.0x gain
			TSEN										Thermal shutdown enable protects chip from thermal destruction on overload 0 = disable thermal shutdown (engineering purposes, only) 1 = enable (default) strongly recommended for normal operation
			AOUTIMP										Output resistance control option for tie-off of unused or disabled outputs. Unused outputs tie to internal voltage reference for reduced pops and clicks. 0 = nominal tie-off impedance value of 1kΩ (default) 1 = nominal tie-off impedance value of 30kΩ
			Default >>	0	0	0	0	0	0	0	1	0	0x002 reset value

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
50	32	Left mixer	LAUXMXGAIN										Gain value between LINPUT auxiliary input and input to LMAIN left output mixer 000 = -15dB (default) 001 = -12dB 010 = -9.0dB 011 = -6.0dB 100 = -3.0dB 101 = 0.0dB 110 = +3.0dB 111 = +6.0dB
			LAUXLMX										LINPUT input to LMAIN left output mixer path control 0 = LINPUT not connected to LMAIN left output mixer (default) 1 = LINPUT connected to LMAIN left output mixer
			Reserved										Reserved
			LDACLMX										Left DAC output to LMIX left output mixer path control 0 = path disconnected (default) 1 = path connected
			Default >>	0	0	0	0	0	0	0	0	1	0x001 reset value
51	33	Right mixer	RAUXMXGAIN										Gain value between LINPUT auxiliary input and input to LMAIN left output mixer 000 = -15dB (default) 001 = -12dB 010 = -9.0dB 011 = -6.0dB 100 = -3.0dB 101 = 0.0dB 110 = +3.0dB 111 = +6.0dB
			RAUXRMX										RINPUT input to RMAIN right output mixer path control 0 = RINPUT not connected to RMAIN right output mixer (default) 1 = RINPUT connected to RMAIN right output mixer
													Reserved
													Reserved
			RDACRMX										Right DAC output to RMIX right output mixer path control 0 = path disconnected (default) 1 = path connected
			Default >>	0	0	0	0	0	0	0	0	1	0x001 reset value
52	34	LHP volume	LHPVU										Headphone output volume update bit feature. Write-only bit for synchronized changes of left and right headphone amplifier output settings If logic = 0 on R52 write, new R52 value stored in temporary register If logic = 1 on R52 write, new R52 and pending R53 values become active
			LHPZC										Left channel input zero cross detection enable 0 = gain changes to left headphone happen immediately (default) 1 = gain changes to left headphone happen pending zero crossing logic
			LHPMUTE										Left headphone output mute control 0 = headphone output not muted, normal operation (default) 1 = headphone in muted condition not connected to LMIX output stage
			LHPGAIN										Left channel headphone output volume control setting. Setting becomes active when allowed by zero crossing and/or update bit features. 11 1001 = 0.0dB default setting 00 0000 = -57dB 00 0001 = -56dB - volume changes in 1.0dB steps per binary bit value – 11 1110 = +5.0dB 11 1111 = +6.0dB
			Default >>	0	0	0	1	1	1	0	0	1	0x039 reset value

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
53	35	**RHP volume**	RHPVU										Headphone output volume update bit feature. Write-only bit for synchronized changes of left and right headphone amplifier output settings If logic = 0 on R53 write, new R53 value stored in temporary register If logic = 1 on R53 write, new R53 and pending R52 values become active
			RHPZC										Right channel input zero cross detection enable 0 = gain changes to right headphone happen immediately (default) 1 = gain changes to right headphone happen pending zero crossing logic
			RHPMUTE										Right headphone output mute control 0 = headphone output not muted, normal operation (default) 1 = headphone in muted condition not connected to RMIX output stage
			RHPGAIN										Right channel headphone output volume control setting. Setting becomes active when allowed by zero crossing and/or update bit features. 11 1001 = 0.0dB default setting 00 0000 = -57dB 00 0001 = -56dB - volume changes in 1.0dB steps per binary bit value – 11 1110 = +5.0dB 11 1111 = +6.0dB
			Default >>	0	0	0	1	1	1	0	0	1	0x039 reset value
54	36	**LSPKOUT volume**	LSPKVU										Loudspeaker output volume update bit feature. Write-only bit for synchronized changes of left and right headphone amplifier output settings If logic = 0 on R54 write, new R54 value stored in temporary register If logic = 1 on R54 write, new R54 and pending R55 values become active
			LSPKZC										Left loudspeaker LSPKOUT output zero cross detection enable 0 = gain changes to left loudspeaker happen immediately (default) 1 = gain changes to left loudspeaker happen pending zero crossing logic
			LSPKMUTE										Right loudspeaker LSPKOUT output mute control 0 = loudspeaker output not muted, normal operation (default) 1 = loudspeaker in muted condition
			LSPKGAIN										Left loudspeaker output volume control setting. Setting becomes active when allowed by zero crossing and/or update bit features. 11 1001 = 0.0dB default setting 00 0000 = -57dB 00 0001 = -56dB - volume changes in 1.0dB steps per binary bit value – 11 1110 = +5.0dB 11 1111 = +6.0dB
			Default >>	0	0	0	1	1	1	0	0	1	0x039 reset value
55	37	**RSPKOUT volume**	RSPKVU										Loudspeaker output volume update bit feature. Write-only bit for synchronized changes of left and right headphone amplifier output settings If logic = 0 on R55 write, new R55 value stored in temporary register If logic = 1 on R55 write, new R55 and pending R54 values become active
			RSPKZC										Right loudspeaker RSPKOUT output zero cross detection enable 0 = gain changes to right loudspeaker happen immediately (default) 1 = gain changes to right loudspeaker happen pending zero crossing logic
			RSPKMUTE										Right loudspeaker RSPKOUT output mute control 0 = loudspeaker output not muted, normal operation (default) 1 = loudspeaker in muted condition
			RSPKGAIN										Right loudspeaker output volume control setting. Setting becomes active when allowed by zero crossing and/or update bit features. 11 1001 = 0.0dB default setting 00 0000 = -57dB 00 0001 = -56dB - volume changes in 1.0dB steps per binary bit value – 11 1110 = +5.0dB 11 1111 = +6.0dB
			Default >>	0	0	0	1	1	1	0	0	1	0x039 reset value

Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
56	38	AUX2 MIXER	Reserved										Reserved
			AUXOUT2MT										AUXOUT2 output mute control 0 = output not muted, normal operation (default) 1 = output in muted condition
			Reserved										Reserved
			AUX1MIX>2										AUX1 Mixer output to AUX2 MIXER input path control 0 = path not connected 1 = path connected
			Reserved										Reserved
			LMIXAUX2										Left LMAIN MIXER output to AUX2 MIXER input path control 0 = path not connected 1 = path connected
			LDACAUX2										Left DAC output to AUX2 MIXER input path control 0 = path not connected 1 = path connected
			Default >>	0	0	0	0	0	0	0	0	1	0x001 reset value
57	39	AUX1 MIXER											Reserved
			AUXOUT1MT										AUXOUT1 output mute control 0 = output not muted, normal operation (default) 1 = output in muted condition
			AUX1HALF										AUXOUT1 6dB attenuation enable 0 = output signal at normal gain value (default) 1 = output signal attenuated by 6.0dB
			LMIXAUX1										Left LMAIN MIXER output to AUX1 MIXER input path control 0 = path not connected 1 = path connected
			LDACAUX1										Left DAC output to AUX1 MIXER input path control 0 = path not connected 1 = path connected
			Reserved										Reserved
			RMIXAUX1										Right RMIX output to AUX1 MIXER input path control 0 = path not connected 1 = path connected
			RDACAUX1										Right DAC output to AUX1 MIXER input path control 0 = path not connected 1 = path connected
			Default >>	0	0	0	0	0	0	0	0	1	0x001 reset value
58	3A	Power Management 4	LPDAC										Reduce DAC supply current 50% in low power operating mode 0 = normal supply current operation (default) 1 = 50% reduced supply current mode
			Reserved										Reserved
			LPSPKD										Reduce loudspeaker amplifier supply current 50% in low power operating mode 0 = normal supply current operation (default) 1 = 50% reduced supply current mode
			PRGREFM										Programmable reference voltage output impedance control 0 = low-Z output impedance mode 1 = approx. 200-ohm output impedance mode
			REGVOLT										Regulator voltage control power reduction options 00 = normal 1.80Vdc operation (default) 01 = 1.61Vdc operation 10 = 1.40 Vdc operation 11 = 1.218 Vdc operation
			IBADJ										Master bias current power reduction options 00 = normal operation (default) 01 = 25% reduced bias current from default 10 = 14% reduced bias current from default 11 = 25% reduced bias current from default
			Default >>	0	0	0	0	0	0	0	0	0	0x000 reset value

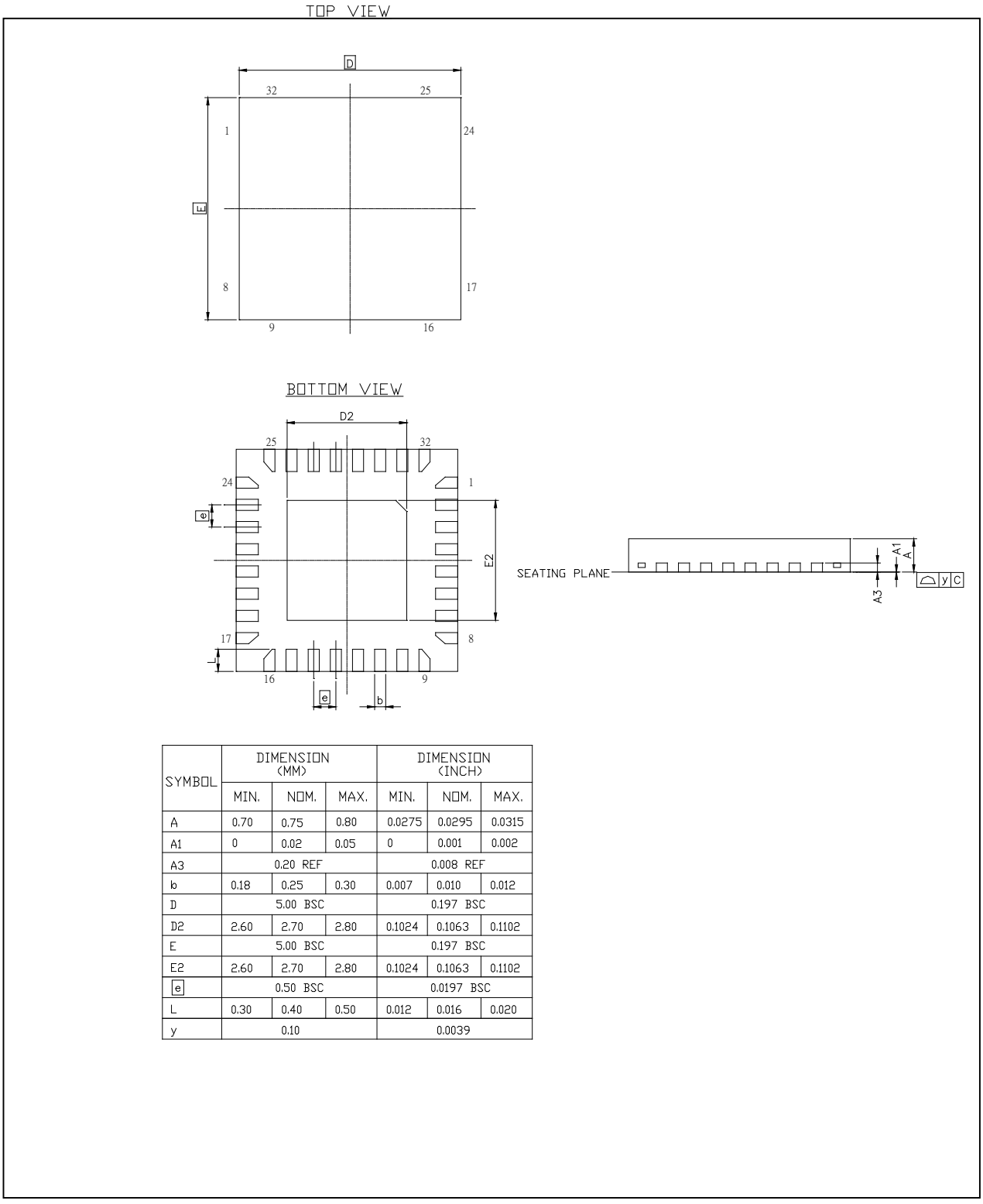
Register		Function	Name	Bit								Description
Dec	Hex			8	7	6	5	4	3	2	1	0	
59	3B	Left time slot	LTSLOT[8:0]										Left channel PCM time slot start count: LSB portion of total number of bit times to wait from frame sync before clocking audio channel data. LSB portion is combined with MSB from R60 to get total number of bit times to wait.
			Default >>	0	0	0	0	0	0	0	0	0	0x000 reset value
60	3C	Misc.	PCMTSEN										Time slot function enable for PCM mode.
			Reserved										
			PCM8BIT										8-bit word length enable
			Reserved										
			RTSLOT[9]										Right channel PCM time slot start count: MSB portion of total number of bit times to wait from frame sync before clocking audio channel data. MSB is combined with LSB portion from R61 to get total number of bit times to wait.
			LTSLOT[9]										Left channel PCM time slot start count: MSB portion of total number of bit times to wait from frame sync before clocking audio channel data. MSB is combined with LSB portion from R59 to get total number of bit times to wait.
			Default >>	0	0	0	1	0	0	0	0	0	0x020 reset value
61	3D	Right time slot	RTSLOT[8:0]										Right channel PCM time slot start count: LSB portion of total number of bit times to wait from frame sync before clocking audio channel data. LSB portion is combined with MSB from R60 to get total number of bit times to wait.
			Default >>	0	0	0	0	0	0	0	0	0	0x000 reset value
62	3E	Device Revision Number	Reserved										Reserved
			REV										Device Revision Number for readback over control interface = read-only value
			Default >>	x	x	x	x	x	x	x	x	x	
63	3F	Device ID#	ID	x	x	x	x	x	x	x	x	x	7-bit Device ID Number for readback over control interface = read-only value
			Default >>	0	0	0	0	1	1	0	1	0	0x01A reset value (read only)

14 Appendix D: Register Overview

DEC	HEX	NAME	Bit 8	Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0	00	Software Reset	RESET (SOFTWARE)									
1	01	Power Management 1	DCBUFEN	AUX1MXEN	AUX2MXEN	PLLEN	PRGREFEN	ABIASEN	IOBUFEN	REFIMP		000
2	02	Power Management 2	RHPEN	NHPEN	SLEEP	Reserved						000
3	03	Power Management 3	AUXOUT1EN	AUXOUT2EN	LSPKEN	RSPKEN	BIASGEN	RMIXEN	LMIXEN	RDACEN	LDACEN	000
General Audio Controls												
4	04	Audio Interface	BCLKP	LRP	WLEN		AIFMT		DACPHS	Reserved	MONO	050
5	05	Companding	Reserved			CMB8	DACCM		Reserved		Reserved	000
6	06	Clock Control 1	CLKM	MCLKSEL			BCLKSEL			Reserved	CLKIOEN	140
7	07	Clock Control 2	4WSPIEN	Reserved				SMPLR			SCLKEN	000
8	08	GPIO	Reserved			GPIO1PLL		GPIO1PL	GPIO1SEL			000
9	09	Jack Detect 1	JCKMIDEN		JCKDEN	JCKDIO		Reserved				000
10	0A	DAC Control	Reserved		SOFTMT	Reserved		DACOS	AUTOMT	RDACPL	LDACPL	000
11	0B	Left DAC Volume	LDACVU	LDACGAIN								0FF
12	0C	Right DAC Volume	RDACVU	RDACGAIN								0FF
13	0D	Jack Detect 2	Reserved	JCKDOEN1				JCKDOEN0				000
14	0E	Reserved										
15	F	Reserved										
16	10	Reserved										
17	11	Reserved										
18	12	EQ1-low cutoff	EQM	Reserved	EQ1CF		EQ1GC					12C
19	13	EQ2-peak 1	EQ2BW	Reserved	EQ2CF		EQ2GC					02C
20	14	EQ3-peak 2	EQ3BW	Reserved	EQ3CF		EQ3GC					02C
21	15	EQ4-peak3	EQ4BW	Reserved	EQ4CF		EQ4GC					02C
22	16	EQ5-high cutoff	Reserved		EQ5CF		EQ5GC					02C
23	17	Reserved										
DAC Limiter												
24	18	DAC Limiter 1	DACLIMEN	DACLIMDCY				DACLIMATK				032
25	19	DAC Limiter 2	Reserved		DACLIMTHL			DACLIMBST				000
26	1A	Reserved										
27	1B	Reserved										
28	1C	Reserved										
29	1D	Reserved										
30	1E	Reserved										
31	1F	Reserved										
Reserved												
32	20	Reserved										
33	21	Reserved										
34	22	Reserved										
35	23	Reserved										
Phase Locked Loop												
36	24	PLL N	Reserved				PLLMCLK	PLLN				008
37	25	PLL K 1	Reserved			PLLK[23:18]						00C
38	26	PLL K 2	PLLK[17:9]									093
39	27	PLL K 3	PLLK[8:0]									0E9
40	28	ProgRef Mode	Reserved								PRGREFM	000
Miscellaneous												
41	29	3D control	Reserved					3DDEPTH				000
42	2A	Reserved										
43	2B	Right Speaker Submix	Reserved			RMIXMUT	RSUBBYP	RAUXRSUBG			RAUXSMUT	000
44	2C	Input Control	PRGREFV		Reserved							033
45	2D	Reserved										
46	2E	Reserved										
47	2F	Reserved										
48	30	Reserved										
49	31	Output Control	Reserved		LDACRMX	RDACLMX	AUX1BST	AUX2BST	SPKBST	TSEN	AOUTIMP	002
50	32	Left Mixer	LAUXMXGAIN			LAUXLMX	Reserved			Reserved	LDACLMX	001
51	33	Right Mixer	RAUXMXGAIN			RAUXRMX	Reserved			Reserved	RDACRMX	001
52	34	LHP Volume	LHPVU	LHPZC	LHPMUTE	LHPGAIN						039
53	35	RHP Volume	RHPVU	RHPZC	RHPMUTE	RHPGAIN						039
54	36	LSPKOUT Volume	LSPKVU	LSPKZC	LSPKMUTE	LSPKGAIN						039
55	37	RSPKOUT Volume	RSPKVU	RSPKZC	RSPKMUTE	RSPKGAIN						039
56	38	AUX2 Mixer	Reserved		AUXOUT2MT	Reserved		AUX1MIX>2	Reserved	LMIXAUX2	LDACAUX2	001
57	39	AUX1 Mixer	Reserved		AUXOUT1MT	AUX1HALF	LMIXAUX1	LDACAUX1	Reserved	RMIXAUX1	RDACAUX1	001
58	3A	Power Management 4	LPDAC	LPIPBST	Reserved	LPSPKD	PRGREFM	REGVOLT		IBADJ		000
PCM Time Slot Controls												
59	3B	Left Time Slot	LTSLOT[8:0]									000
60	3C	Misc	PCMTSEN	Reserved	PCM8BIT	Reserved	Reserved	Reserved	Reserved	RTSLOT[9]	LTSLOT[9]	020
61	3D	Right Time Slot	RTSLOT[8:0]									000
Silicon Revision and Device ID												
62	3E	Device Revision #	REV									xxx
63	3F	Device ID	ID									01A

15 Package Dimensions

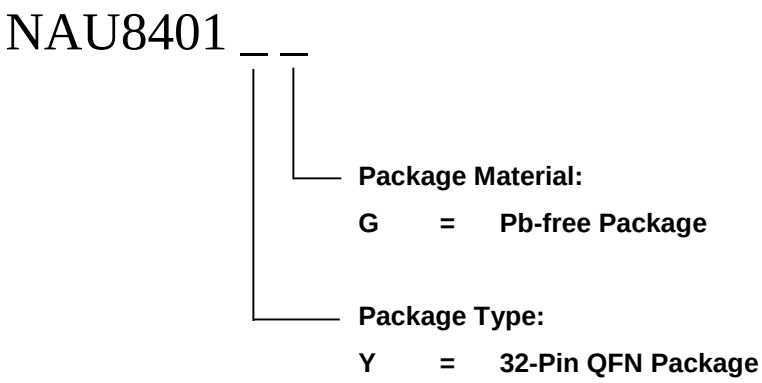
32-lead plastic QFN 32L; 5X5mm^2, 0.8mm thickness, 0.5mm lead pitch



SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0275	0.0295	0.0315
A1	0	0.02	0.05	0	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	5.00 BSC			0.197 BSC		
D2	2.60	2.70	2.80	0.1024	0.1063	0.1102
E	5.00 BSC			0.197 BSC		
E2	2.60	2.70	2.80	0.1024	0.1063	0.1102
e	0.50 BSC			0.0197 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
y	0.10			0.0039		

16 Ordering Information

Part Number	Dimension	Package	Package Material
NAU8401YG	5x5 mm	QFN-32	Green



REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A0.0	Dec. 15, 2008	n/a	Initial Version
V1.0	Feb. 12, 2008	n/a	Various minor changes for v1.0
V1.1	March 15, 2010	n/a	Updated package information and general update
V1.2	April 20, 2010	1, 4	Diagram updated
V1.3	July 19, 2010	all	Unified appearance, fix R04 erratum, and minor text edits
V2.0	January 25, 2011	14 48	Corrected location of low power mic bias bit from R40 to R58 Included Power Management 2 in Table
V2.1	October 2013	45 8	Corrected 2 wire interface timing diagram Corrected Digital I/O voltage levels from DCVDD to DBVDD
V2.2	March 2014	7 31 32 42 43	Corrected SPKOUT and AUXOUT full scale output Modified 2-wire write figure Modified 2-wire read figure Corrected rising/falling time specification of I2S Modified application circuit
V2.3	Nov. 2014	41	Corrected Tsdios setup time
V2.4	Jan. 2015	1	Updated AECQ100 description
V2.5	March 2016	20	Add Important Notice
V2.6	July 2018	27 43	Revise equation from * to / I2C low pass filter

Table 17: Revision History

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.

Please note that all data and specifications are subject to change without notice.
All the trademarks of products and companies mentioned in this datasheet belong to their respective owners.