LC²MOS Analog I/O Port

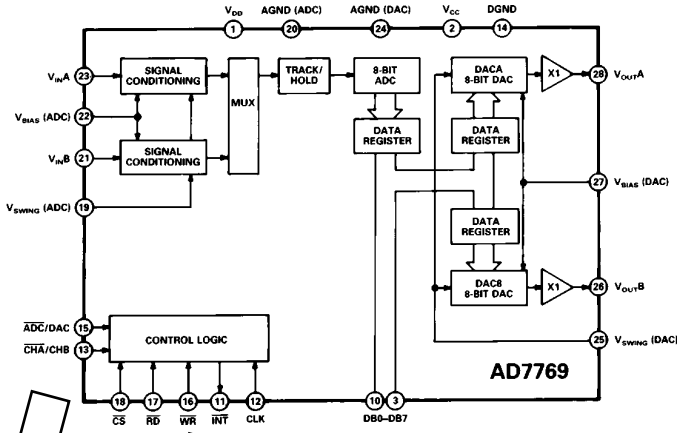
AD7769*

FEATURES
Two-Channel, 8-Bit 2.5 μs ADC
Two 8-Bit, 2.5 μs DACs with Output Amplifiers
Span and Offset of ADC and DAC Independently Adjustable
Low Power

APPLICATIONS
Winchester Disk Servo Controllers
Floppy Disk Microstepping
Closed Loop Servo Systems

OBSOLETE

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7769 is a complete, two-channel, 8-bit, analog I/O port. It has versatile input and output signal conditioning features that make it ideal for use in head-positioning servos in Winchester disk systems. It is equally suitable for floppy disk microstepping head positioning, other closed loop digital servo systems and general purpose 8-bit data acquisition.

The AD7769 contains a high speed successive approximation ADC, preceded by a two-channel multiplexer and signal conditioning circuits. The input span of the ADC and the offset of the zero point from ground can be independently set by applying ground referenced voltages. The AD7769 also contains two independent, fast settling, 8-bit DACs with output amplifiers. The output span and offset voltage of the DACs can be set independently of those of the ADC. This makes the AD7769 especially useful in disk drives, where only a positive supply rail is available and the ranges of the ADC and DACs must be referenced to some positive voltage less than the supply.

The AD7769 is easily interfaced to a standard 8-bit mpu bus via an 8-bit data port and standard microprocessor control lines.

The AD7769 is fabricated in Linear Compatible CMOS (LC^2MOS), an advanced, mixed technology process that combines precision bipolar circuits with low power CMOS logic. The part is available in a 28-pin plastic DIP and 28-terminal PLCC package.

***Covered by U.S. Patent No. 4,990,916.**

PRODUCT HIGHLIGHTS

1. Two-Channel, 8-Bit Analog I/O port on a Single Chip.
   The AD7769 contains a two-channel, high speed ADC with input signal conditioning and two, fast settling 8-bit DACs with output amplifiers, on a single chip.
2. Independent Control of Span and Offset.
   The input voltage span of the ADC and the midpoint of the transfer function, the output voltage swing of the two DACs and the half-scale output voltage, can be set independently by applying ground referenced control voltages.
3. Dynamic Specifications for DSP Users.
   In addition to the traditional ADC and DAC specifications, the AD7769 is specified with ac parameters including signal-to-noise ratio, distortion and signal bandwidth.
4. Fast Microprocessor Interface.
   The AD7669 has bus interface timing compatible with all modern microprocessors, with bus access and relinquish times less than 65 ns and a Write pulse width less than 90 ns.

REV. A

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AD7769–SPECIFICATIONS

ADC SPECIFICATIONS (V_{DD} = +12 V ± 10%; V_{CC} = +5 V ± 5%; AGND [ADC] = AGND [DAC] = DGND = 0 V; V_{BIAS} [ADC] = +5 V; V_{SWING} [ADC] = +2.5 V; f_{CLK} = 5 MHz external. All specifications T_{MIN} to T_{MAX}[1] unless otherwise noted.)

Parameter	J Version	A Version	Units	Conditions/Comments
DC ACCURACY				
Resolution	8	*	Bits	
Relative Accuracy	±1	*	LSB max	See Terminology
Differential Nonlinearity	±1	*	LSB max	No Missing Codes. See Terminology.
Bias Offset Error				See Terminology
+25°C	±2.5	*	LSB max	
T_{MIN} to T_{MAX}	±3.0	*	LSB max	
Bias Offset Match				Channel A to Channel B
+25°C	±2.5	*	LSB max	
T_{MIN} to T_{MAX}	±3.5	*	LSB max	
Plus or Minus Full-Scale Error				See Terminology
+25°C	±2.0	*	LSB max	
T_{MIN} to T_{MAX}	±2.5	*	LSB max	
Plus or Minus Full-Scale Match				Channel A to Channel B
+25°C	±3.5	*	LSB max	
T_{MIN} to T_{MAX}	±4	*	LSB max	
ADC TO DAC MATCHING				Channel A/B to V_{OUT} A/B
Bias Offset Match				V_{BIAS} (DAC) = +5 V, V_{SWING} (DAC) = +2.5 V.
+25°C	±2.5	*	LSB max	
T_{MIN} to T_{MAX}	±3.5	*	LSB max	
Plus or Minus Full-Scale Match				
+25°C	±3.5	*	LSB max	
T_{MIN} to T_{MAX}	±4.0	*	LSB max	
DYNAMIC PERFORMANCE[2]				
Signal-to-Noise Ratio (SNR)	44	*	dB min	V_{IN} = 100 kHz Full-Scale Sine Wave with $f_{SAMPLING}$ = 400 kHz
Total Harmonic Distortion (THD)	48	*	dB max	V_{IN} = 100 kHz Full-Scale Sine Wave with $f_{SAMPLING}$ = 400 kHz
Intermodulation Distortion (IMD)	60	*	dB typ	f_a = 99 kHz, f_b = 96.7 kHz with $f_{SAMPLING}$ = 400 kHz
Frequency Response	0.1	*	dB typ	V_{IN} = Full-Scale, dc to 200 kHz Sine Wave
ANALOG INPUTS				
Input Voltage Ranges, $V_{IN}A$, $V_{IN}B$	V_{BIAS} – V_{SWING} or 0		V min	Whichever Is the Higher
	V_{BIAS} + V_{SWING} or 9.8		V max	Whichever Is the Lower
Input Currents, $I_{IN}A$, $I_{IN}B$	±0.4	*	mA max	
ADC REFERENCE INPUTS				
Input Voltage Levels				
V_{BIAS} (ADC)	2/6.8	*	V min/max	With Respect to AGND (ADC). For Specified Performance.
V_{SWING} (ADC)	2.0/3.0	*	V min/max	With Respect to AGND (ADC). For Specified Performance.
Input Currents				
V_{BIAS} (ADC) Input	±800	*	µA max	
V_{SWING} (ADC) Input	±1	*	µA max	
LOGIC OUTPUTS				
DB0–DB7, $\overline{INT}$				
V_{OL}, Output Low Voltage	0.4	*	V max	I_{SINK} = 1.6 mA
V_{OH}, Output High Voltage	4.0	*	V min	I_{SOURCE} = 200 µA
DB0–DB7				
Floating State Leakage Current	±10	*	µA max	
Floating State Capacitance[2]	10	*	pF max	
Output Coding	Offset Binary			
POWER REQUIREMENTS				
V_{CC} Range	4.75/5.25	*	V min/V max	For Specified Performance. The Part Will Function with V_{CC} = 5 V ±10% with Degraded Performance.
V_{DD} Range	10.8/13.2	*	V min/V max	For Specified Performance
I_{DD} @ +25°C	20	*	mA max	For ADC and DAC: V_{BIAS} = 5.0 V; V_{SWING} = 3.0 V; $V_{IN}A$,
$V_{UB}Am$ $V_{IN}B$ = T_{MIN} to T_{MAX}	22	*	mA max	V_{BIAS}; DAC Code = FF (Hex); DACA and DACB Load = 5 kΩ to AGND (DAC). Typically I_{DD} = 14 mA.
I_{CC} @ +25°C	5	*	mA max	Logic Inputs = 2.4 V, CLK Input = 0.8 V. Typically I_{CC} =
T_{MIN} to T_{MAX}	6	*	mA max	1.5 mA.

OBSOLETE

NOTES
[1] Temperature range as follows: J Version: 0°C to +70°C; A Version: –40°C to +85°C.
[2] Sample tested at +25°C to ensure compliance.
*Specification same as J Version.
Specifications subject to change without notice.

DACA, DACB SPECIFICATIONS

(V_{DD} = +12 V ± 10%; V_{CC} = +5 V ± 5%; AGND [DAC] = AGND [ADC] = DGND = 0 V; V_{BIAS} [DAC] = +5 V; V_{SWING} [DAC] = +2.5 V; V_{OUT}A, V_{OUT}B load to AGND [DAC], R_L = 5 kΩ, C_L = 100 pF. All specifications T_{MIN} to T_{MAX}[1] unless otherwise noted.)

Parameter	J Version	A Version	Units	Conditions/Comments
STATIC PERFORMANCE				
Resolution	8	*	Bits	
Relative Accuracy	±1	*	LSB max	See Terminology
Differential Nonlinearity	±1	*	LSB max	Guaranteed Monotonic. See Terminology.
Bias Offset Error				See Terminology
+25°C	±2.0	*	LSB max	
T_{MIN} to T_{MAX}	±2.5	*	LSB max	
Bias Offset Match				V_{OUT} A to V_{OUT} B
+25°C	±2.5	*	LSB max	
T_{MIN} to T_{MAX}	±3.5	*	LSB max	
Plus or Minus Full-Scale Error				See Terminology
+25°C	±1.5	*	LSB max	
T_{MIN} to T_{MAX}	±2.0	*	LSB max	
Plus or Minus Full-Scale Match				V_{OUT} A to V_{OUT} B
+25°C	±3.5	*	LSB max	
T_{MIN} to T_{MAX}	±4.0	*	LSB max	
ADC to DAC MATCHING	As Per ADC Specifications			
DYNAMIC PERFORMANCE[2]				
Signal-to-Noise Ratio (SNR)	44	*	dB min	V_{OUT} = 20 kHz Full-Scale Sine Wave With $f_{SAMPLING}$ = 400 kHz
Total Harmonic Distortion (THD)	48	*	dB max	V_{OUT} = 20 kHz Full-Scale Sine Wave With $f_{SAMPLING}$ = 400 kHz
Intermodulation Distortion (IMD)	55	*	dB typ	f_a = 18.4 kHz, f_b = 14.5 kHz with $f_{SAMPLING}$ = 400 kHz
ANALOG OUTPUTS				
Output Voltage Ranges				
V_{OUT}A, V_{OUT}B	$V_{BIAS} - V_{SWING}$ or 0.5		V min	Whichever Is the Higher
	$V_{BIAS} + V_{SWING}$ or V_{DD} –2.0		V max	Whichever Is the Lower
DC Output Impedance	0.5	*	Ω typ	
Short-Circuit Current	20	*	mA typ	
DAC REFERENCE INPUTS				
Input Voltage Levels				
V_{BIAS} (DAC)	3/6.8	*	V min/max	With Respect to AGND (DAC). For Specified Performance.
V_{SWING} (DAC)	2.0/3.0	*	V min/max	With Respect to AGND (DAC). For Specified Performance.
Input Currents				
V_{BIAS} (DAC) Input	±2	*	µA max	
V_{SWING} (DAC) Input	±1	*	µA max	
AC CHARACTERISTICS[2]				
Voltage Output Settling Time	4	*	µs max	Settling Time to Within ±1/2 LSB of Final Value. Typically 2.5 µs.
Digital-to-Analog Glitch Impulse	30	*	nV sec typ	See Terminology
Digital Feedthrough	1	*	nV sec typ	See Terminology
LOGIC INPUTS				
$\overline{CS}$, RD, $\overline{WR}$, $\overline{ADC}$/DAC, $\overline{CHA}$/CHB, DB0–DB7				
Input Low Voltage, V_{INL}	0.8	*	V max	
Input High Voltage, V_{INH}	2.4	*	V min	
Input Leakage Current	±10	*	µA max	
Input Capacitance	10	*	pF max	
CLK				
Input Low Voltage	0.8	*	V max	External Clock. For Internal Clock Operation Connect
Input High Voltage	2.4	*	V min	the CLK Pin to V_{DD}.
Input Leakage Current	±10	*	µA max	
DB0–DB7				
Input Coding	Offset Binary			
POWER REQUIREMENTS	As per ADC Specifications			

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NOTES

[1]Temperature range as follows: J Version: 0°C to +70°C; A Version: –40°C to +85°C.

[2]Sample tested at +25°C to ensure compliance.

*Specifications same as J Version.

Specifications subject to change without notice.

AD7769

TIMING CHARACTERISTICS[1, 2] (V_{CC} = +5 V ± 5%; V_{DD} = +12 V ± 10%; AGND [ADC] = AGND [DAC] = DGND = 0 V. For ADC and DAC, V_{BIAS} = +5 V, V_{SWING} = +2.5 V.)

Parameter	Label	Limit at +25°C	Limit at T_{MIN}, T_{MAX}	Units	Test Conditions/Comments
ADC /DAC CONTROL TIMING					
$\overline{CS}$ to $\overline{WR}$ Setup Time	t_1	0	0	ns min	
$\overline{CS}$ to $\overline{WR}$ Hold Time	t_2	0	0	ns min	
$\overline{ADC}$/DAC to $\overline{WR}$ Setup Time	t_3	0	0	ns	
$\overline{ADC}$/DAC to $\overline{WR}$ Hold Time	t_4	0	0	ns min	
$\overline{CHA}$/CHB to $\overline{WR}$ Setup Time	t_5	0	0	ns min	
$\overline{CHA}$/CHB to $\overline{WR}$ Hold Time	t_6	0	0	ns min	
$\overline{WR}$ Pulse Width	t_7	80	80	ns min	
ADC CONVERSION TIMING					
Using External Clock					Load Circuit of Figure 3, C_L = 20 pF
$\overline{WR}$ to $\overline{INT}$ Low Delay	t_8	2.6	2.6	µs max	
Using Internal Clock					Load Circuit of Figure 3, C_L = 20 pF
$\overline{WR}$ to $\overline{INT}$ Low Delay	t_8	1.9/3.0	1.9/3.0	µs min/max	Typically 2.5 µs
$\overline{WR}$ to $\overline{INT}$ High Delay	t_9	85	85	ns max	Load Circuit of Figure 3, C_L = 20 pF
	t_9	120	120	ns max	Load Circuit of Figure 3, C_L = 100 pF
$\overline{WR}$ to Data Valid Delay[3]	t_{10}	t_8+70	t_8+70	ns max	Load Circuit of Figure 1, C_L = 20 pF
	t_{10}	t_8+110	t_8+110	ns max	Load Circuit of Figure 1, C_L = 100 pF
ADC READ TIMING					
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_{11}	0	0	ns min	
$\overline{CS}$ to $\overline{RD}$ Hold Mode	t_{12}	0	0	ns min	
$\overline{RD}$ to Data Valid Delay[3]	t_{13}	15/65	15/65	ns min/max	Load Circuit of Figure 1, C_L = 20 pF
	t_{13}	30/100	30/100	ns min/max	Load Circuit of Figure 1, C_L = 100 pF
Bus Relinquish Time after $\overline{RD}$ High[4]	t_{14}	15/65	15/65	ns min/max	Load Circuit of Figure 2
$\overline{RD}$ to $\overline{INT}$ High Delay	t_{15}	80	80	ns max	Load Circuit of Figure 3, C_L = 20 pF
	t_{15}	110	110	ns max	Load Circuit of Figure 3, C_L = 100 pF
$\overline{RD}$ Pulse Width	t_{16}	t_{13}	t_{13}	ns min	Determined by t_{13}
DAC WRITE TIMING					
Data Valid to $\overline{WR}$ Setup Time	t_{17}	65	65	ns min	
Data Valid to $\overline{WR}$ Hold Time	t_{18}	15	20	ns min	
$\overline{WR}$ to DAC Output Settling Time	t_{19}	4	4	µs max	Load Circuit of Figure 4

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NOTES

[1]See Figures 11, 12 and 13.

[2]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

[3]t_{10} and t_{13} are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.

[4]t_{14} is defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 2.

Specifications subject to change without notice.

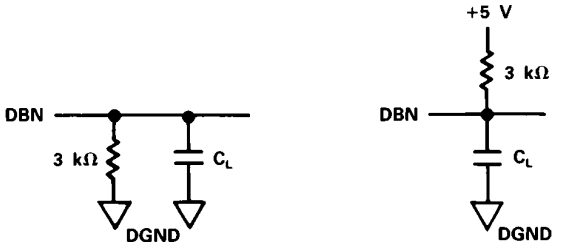

Figure 1. Load Circuits for Data Access Time Test

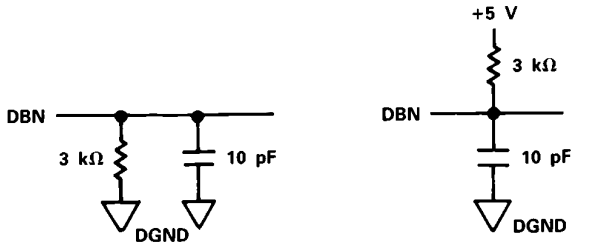

Figure 2. Load Circuits for Bus Relinquish Time Test

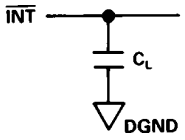

Figure 3. Load Circuit for $\overline{RD}$ and $\overline{WR}$ to $\overline{INT}$ Delay Test

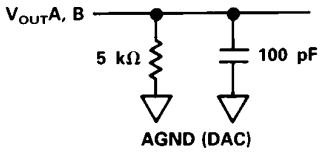

Figure 4. Load Circuit for DAC Settling Time Test

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND or DGND . . . . . –0.3 V, +15 V
V_{CC} to DGND . . . . . –0.3 V, V_{DD} +0.3 V or 7 V (Whichever is Lower)
AGND to DGND . . . . . –0.3 V, V_{DD} +0.3 V
Digital Inputs to DGND
(Pins 12, 13, 15–18) . . . . . –0.3 V, V_{DD} +0.3 V
Digital Outputs to DGND
(Pins 3–10, 11) . . . . . –0.3 V, V_{CC} +0.3 V
Analog Inputs to AGND . . . . . –0.3 V, V_{DD} +0.3 V
Analog Outputs to AGND . . . . . –0.3 V, V_{DD} +0.3 V
Operating Temperature Range
Commercial (J Version) . . . . . 0°C to +70°C
Industrial (A Version) . . . . . –40°C to +85°C
Power Dissipation (Any Package)
to +75°C . . . . . 500 mW
Derates Above +75°C by . . . . . 6 mW/°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering 10 secs) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one Absolute Maximum Rating may be applied at any one time.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7769 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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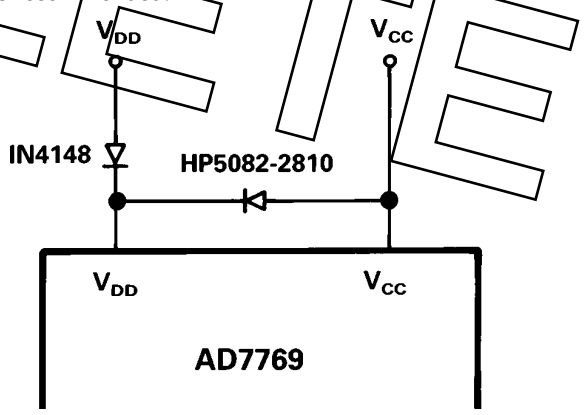
ORDERING GUIDE

Model	Temperature Range	Package Option*
AD7769JN	0°C to +70°C	N-28
AD7769JP	0°C to +70°C	P-28A
AD7769AN	–40°C to +85°C	N-28
AD7769AP	–40°C to +85°C	P-28A

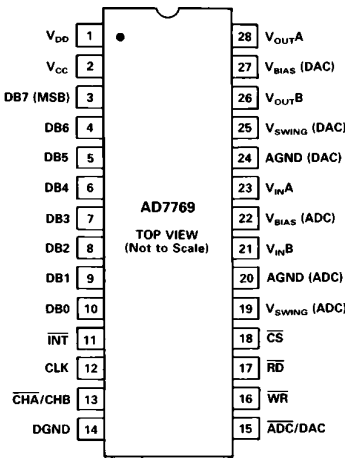
*N = Plastic DIP; P = Plastic Leaded Chip Carrier.

NOTE
Do not allow V_{CC} to exceed V_{DD} by more than 0.3 V. In cases where this can happen the diode protection scheme shown below is recommended.

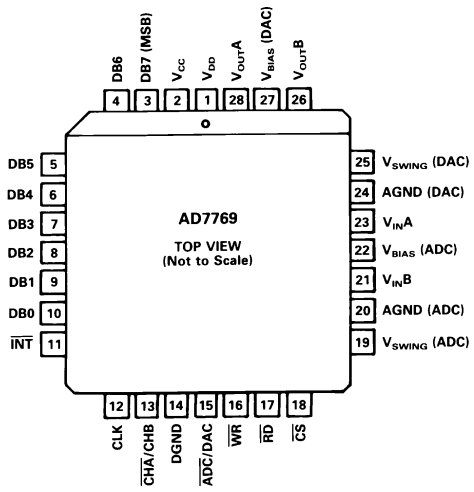


PIN CONFIGURATIONS

DIP



PLCC



PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Description
1	V_{DD}	+12 V Power Supply. This powers the analog circuitry.
2	V_{CC}	+5 V Power Supply. This powers the logic circuitry.
3–10	DB7–DB0	Input/Output Data Bus. A bidirectional data port from which ADC output data may be read and to which DAC input data may be written. DB7 is the Most Significant Bit.
11	$\overline{INT}$	Interrupt Output (active low). $\overline{INT}$ is set high on the falling edge of $\overline{RD}$ or $\overline{WR}$ to the ADC and goes low at the end of a conversion.
12	CLK	Clock input. A clock is required for the ADC. An external TTL-compatible clock may be applied to this input pin. Alternatively, tying this pin to V_{DD} enables the internal clock oscillator. With an external clock, the mark-space ratio can vary from 30/70 to 70/30.
13	$\overline{CHA}$/CHB	Channel A/Channel B Select Input. Selects Channel A or Channel B of the DAC or ADC. Used in conjunction with $\overline{WR}$, $\overline{RD}$, $\overline{CS}$ and $\overline{ADC}$/DAC for read or write operations.
14	DGND	Digital Ground.
15	$\overline{ADC}$/DAC	ADC or DAC Select Input. Selects either the ADC or the DAC for read or write operations in conjunction with $\overline{WR}$, $\overline{RD}$, $\overline{CS}$ and $\overline{CHA}$/CHB.
16	$\overline{WR}$	Write Input (edge triggered). This is used in conjunction with the $\overline{ADC}$/DAC, $\overline{CHA}$/CHB and $\overline{CS}$ control inputs to start an ADC conversion or write data to the DAC. An ADC conversion starts on the rising edge of $\overline{WR}$.
17	$\overline{RD}$	Read Input (active low). This input must be low to access data from the ADC.
18	$\overline{CS}$	Chip Select Input (active low). The device is selected when this input is low.
19	V_{SWING} (ADC)	ADC Reference Input. The voltage applied to this pin with respect to AGND (ADC) sets the in put voltage Full-Scale Range (FSR) of the ADC. V_{IN} (FSR) = 2 V_{SWING} (ADC).
20	AGND (ADC)	ADC Analog Ground.
21	V_{IN}B	Analog Input for Channel B. See V_{IN}A description.
22	V_{BIAS} (ADC)	ADC Reference Input. The voltage applied to this pin with respect to AGND (ADC) sets the midpoint of the ADC transfer function.
23	V_{IN}A	Analog Input for Channel A. The input voltage range of both ADC channels is given by: V_{IN} A/B = V_{BIAS} (ADC) ±V_{SWING} (ADC).
24	AGND (DAC)	DAC Analog Ground.
25	V_{SWING} (DAC)	DAC Reference Input. The voltage applied to this pin with respect to AGND (DAC) sets the output voltage Full-Scale Range (FSR) of the DACs. V_{OUT} (FSR) = 2 V_{SWING} (DAC).
26	V_{OUT}B	Analog Output Voltage from DAC B. See V_{OUT}A description.
27	V_{BIAS} (DAC)	DAC Reference Input. The voltage applied to this pin with respect to AGND (DAC) sets the midpoint output voltage of the DACs.
28	V_{OUT}A	Analog Output Voltage from DAC A. The output voltage range of both DACs is given by: V_{OUT} A/B = V_{BIAS} (DAC) ± V_{SWING} (DAC).

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TERMINOLOGY

Relative Accuracy

For an ADC, Relative Accuracy or endpoint nonlinearity is the maximum deviation, in LSBs, of the ADC's actual code transition points from a straight line drawn between the endpoints of the ADC transfer function, i.e., the 00 to 01 and FE to FF Hex (01111111 to 11111111 Binary) code transitions.

For a DAC, Relative Accuracy or endpoint nonlinearity is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function, i.e., those voltages which correspond to codes 00 and FF Hex.

For the specified input and output ranges, 1 LSB = 19.5 mV, but will vary with V_{SWING}. For both DACs and ADC, 1 LSB = 2 V_{SWING} / 256 = FSR / 256.

Differential Nonlinearity

Differential Nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB max ensures monotonicity (DAC) or no missed codes (ADC).

Bias Offset Error

For an ideal ADC, the output code for an input voltage equal to V_{BIAS} (ADC), should be 80 Hex (10000000 binary). The ADC Bias Offset Error is the difference between the actual midpoint voltage for code 80 Hex and V_{BIAS} (ADC), expressed in LSBs.

For an ideal DAC, the output voltage for code 80 Hex should be equal to V_{BIAS} (DAC). The DAC Bias Offset Error is the difference between the actual output voltage and V_{BIAS} (DAC), expressed in LSBs.

Plus and Minus Full-Scale Error

The ADC and DACs in the AD7769 can be considered as devices with bipolar (plus and minus) input ranges, but referred to V_{BIAS} instead of AGND. Plus Full-Scale Error for the ADC is the difference between the actual input voltage at the FE to FF code transition and the ideal input voltage (V_{BIAS} + V_{SWING} –1.5 LSB), expressed in LSBs. Minus Full-Scale Error is similarly specified for the 01 to 00 code transition, relative to the ideal input voltage for this transition (V_{BIAS} – V_{SWING} +0.5 LSB). Plus Full-Scale Error for the DACs is the difference, expressed in LSBs, between the actual output voltage for input code FF and the ideal voltage (V_{BIAS} + V_{SWING} – 1 LSB). Minus Full-Scale Error is similarly specified for code 00, relative to the ideal output voltage (V_{BIAS} – V_{SWING}). Note that Plus and Minus Full-Scale errors for the ADC and the DAC outputs are measured after their respective Bias Offset errors have been adjusted out.

Digital-to-Analog Glitch Impulse

Digital-to-Analog Glitch Impulse is the impulse injected into the analog outputs when the digital inputs change state with either DAC selected. It is normally specified as the area of the glitch in nV secs and is measured when the digital input code is changed by 1 LSB at the major carry transition.

Digital Feedthrough

Digital Feedthrough is also a measure of the impulse injected into the analog outputs from the digital inputs but is measured when the DACs are not selected. It is essentially feedthrough across the die and package. It is important in the AD7769 since it is a measure of the glitch impulse transferred to the analog outputs when data is read from the ADC register. It is specified in nV secs and is measured with $\overline{WR}$ high and a digital code change from all 0s to all 1s.

Signal-to-Noise Ratio (SNR)

SNR is the measured Signal-to-Noise Ratio at the output of the converter. The signal is the rms magnitude of the fundamental. Noise is the rms sum of all the nonfundamental signals up to half the sampling frequency. SNR is dependent on the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical SNR for a sine wave is given by

$$SNR = (6.02N + 1.76)\ dB$$

where N is the number of bits. Thus for an ideal 8-bit converter, $SNR = 49.92\ dB$.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of harmonics to the fundamental. For the AD7769, Total Harmonic Distortion is defined as

$$20\ log\ \frac{(V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2)^{1/2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, V_5 and V_6 are the rms amplitudes of the individual harmonics.

Intermodulation Distortion (IMD)

With inputs consisting of sine waves at two frequencies, f_a and f_b, any active device with nonlinearities will create distortion products, of order (m+n), at sum and difference frequencies of mf_a+nf_b, where m, n = 0, 1, 2, 3 . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms include (f_a+f_b) and ($f_a–f_b$) and the third order terms include ($2f_a+f_b$), ($2f_a–f_b$), (f_a+2f_b) and ($f_a–2f_b$).

OBSOLETE

LOGIC TRUTH TABLE

ADC CHANNEL SELECT AND START CONVERSION

$\overline{CS}$	$\overline{ADC}$/DAC	$\overline{CHA}$/CHB	$\overline{WR}$	$\overline{RD}$	DB0–DB7	$\overline{INT}$	Comments
0	0	X		Note 1	Note 1	1	$\overline{INT}$ Is Set on Falling Edge of $\overline{WR}$.
0	0	0		Note 1	Note 1	1	Select ADC Channel A and Start Conversion.
0	0	1		Note 1	Note 1	1	Select ADC Channel B and Start Conversion.
						0	$\overline{INT}$ Goes Low at End of Conversion.

READ ADC DATA

$\overline{CS}$	$\overline{ADC}$/DAC	$\overline{CHA}$/CHB	$\overline{WR}$	$\overline{RD}$	DB0–DB7	$\overline{INT}$	Comments
0	X	X	X		ADC Data	1	$\overline{INT}$ Is Set High on Falling Edge of $\overline{RD}$.
0	X	X	X	0	ADC Data	1	ADC Data on Data Bus.
0	X	X	X		High-Z	1	Data Outputs Impedance.

WRITE TO DACA OR DACB

$\overline{CS}$	$\overline{ADC}$/DAC	$\overline{CHA}$/CHB	$\overline{WR}$	$\overline{RD}$	DB0–DB7	$\overline{INT}$	Comments
0	1	0		1	µP Data	N/C	µP Writing Data to DACA.
0	1	1		1	µP Data	N/C	µP Writing Data to DACB.
0	1	0		0	ADC Data	N/C	Data from Last ADC Conversion Will Be Written to DACA.
0	1	1		0	ADC Data	N/C	Data from Last ADC Conversion Will Be Written to DACB.
1	X	X	X	X	High-Z	N/C	No Operation.

NOTES

[1]If $\overline{RD}$ = 1, DB0–DB7 will remain high impedance. If $\overline{RD}$ = 0, DB0–DB7 will output previous ADC data. The $\overline{RD}$ input should not change during a conversion.

[2]X = Don't Care.

[3]N/C = No Change.

CIRCUIT DESCRIPTION

Analog Inputs and Outputs

The AD7769 provides the analog-to-digital and digital-to-analog conversion functions required between the microcontroller and the servo power amplifier in digital servo systems. It is intended primarily for closed loop head positioning in Winchester disk drives but may also be used for microstepping in drives with stepper motor head positioning or other servo applications. The AD7769 contains a high speed, 8-bit, sampling ADC with two input channels and two 8-bit DACs with output buffer amplifiers. A unique feature of the AD7769 is the input and output signal conditioning circuitry which allows the analog input and output voltages to be referred to a point other than analog ground. The input range and offset of the ADC, the output swing and offset of the DACs may be adjusted independently by the application of ground-referenced, positive control voltages, V_{BIAS} (ADC), V_{SWING} (ADC), V_{BIAS} (DAC) and V_{SWING} (DAC). Thus, for example, the peak-to-peak output swing of the DACs could be set to 3 V above and 3 V below a bias voltage of 5 V.

Figures 5 and 6 show the transfer functions of the ADC and DACs and their relationship to V_{BIAS} and V_{SWING}. The mid-point code of the ADC, 80 Hex (10000000 Binary), occurs at an input voltage equal to V_{BIAS}. The input FSR of the ADC is equal to 2 V_{SWING}, so that the Plus Full-Scale code transition (FE to FF Hex) occurs at a voltage equal to V_{BIAS} + V_{SWING} –1.5 LSBs and the Minus Full-Scale code transition (01 to 00 Hex) occurs at a voltage V_{BIAS} – V_{SWING} +0.5 LSBs. The transfer function of the DACs bears a similar relationship to V_{BIAS} and V_{SWING}. The DAC output voltage for code 80 Hex (10000000 binary) is equal to V_{BIAS}, while FF Hex (11111111 binary) gives an output voltage of V_{BIAS} + V_{SWING} –1 LSB (Plus Full-Scale) and 00 Hex gives an output voltage of V_{BIAS} – V_{SWING} (Minus Full-Scale).

The ability to refer input and output signals to some voltage other than ground is of particular importance in disk drive applications. Typically, only +5 V digital and +12 V analog supply voltages are available, and the analog signals are often referred to a voltage around half the analog supply.

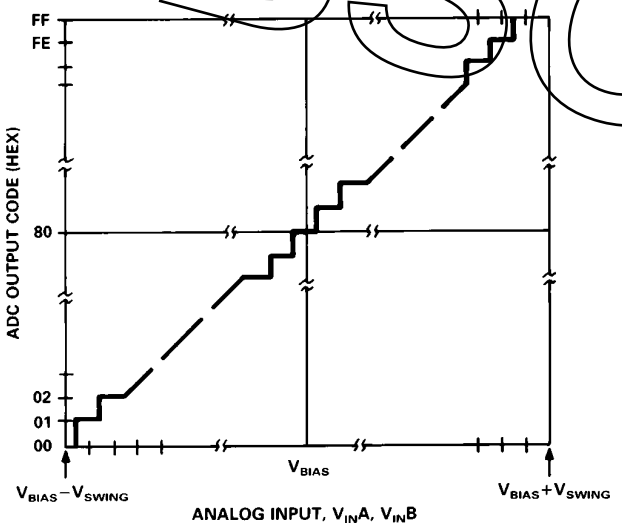


Figure 5. ADC Transfer Function

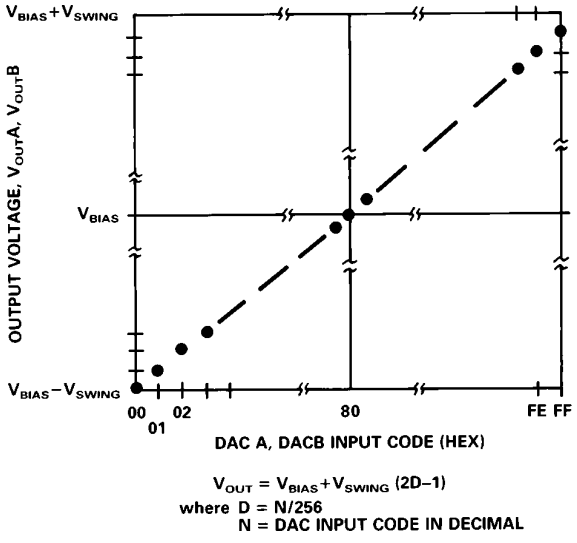


Figure 6. DAC Transfer Function

Driving the Analog Inputs and Reference Inputs

The analog inputs, V_{IN}A and V_{IN}B, must be driven from low output impedance sources, such as from op amps. In addition, V_{BIAS} (ADC) must be driven from a similar type low impedance source (e.g., voltage reference).

Op amps are not required to drive the V_{SWING} (ADC), V_{BIAS} (DAC) and V_{SWING} (DAC) inputs as these are high impedance inputs (200 nA typical input current) that feed into on-chip buffer amplifiers. The reference voltages for these inputs can be derived using suitable resistor divider networks.

The analog reference available in the disk drive system can be used to set the bias voltage of the AD7769, and could also be attenuated to provide the reference for the input and output swing as shown in Figure 7. The same bias voltage would generally (though not necessarily) be used for the ADC and the DACs, though the input and output ranges might be different.

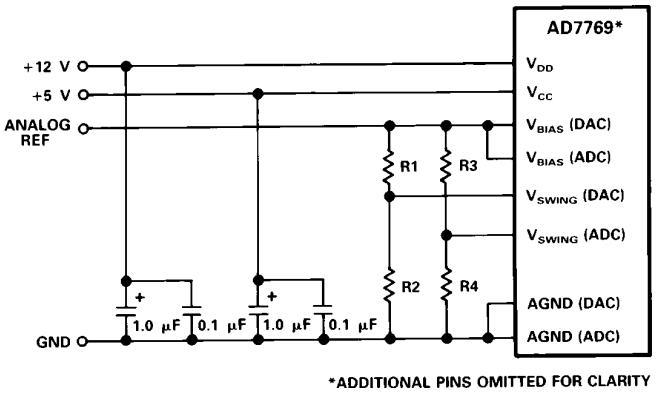


Figure 7. Typical Analog Connections to the AD7769

ADC Conversion Cycle

Figure 8 shows the operating waveforms for a conversion cycle. On the rising edge of $\overline{WR}$, the conversion cycle starts with the acquisition and tracking of the selected ADC channel, V_{IN}A or V_{IN}B. The analog input voltage is held 50 ns (typically) after the fourth falling edge of the input CLK following a conversion start. If t_D in Figure 8 is greater than 150 ns, then the falling edge of the input CLK will be seen as the first falling clock edge. If t_D is less than 150 ns, the first falling clock edge to be recognized will not occur until one cycle later.

OBSOLETE

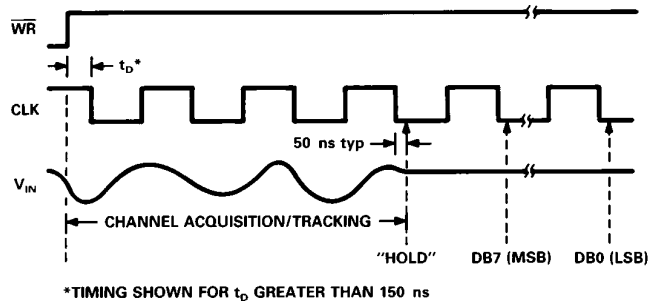


Figure 8. Operating Waveforms Using External Clock

Following the "hold" on the analog input, the MSB decision is made approximately 50 ns after the next falling edge of the input CLK. The succeeding bit decisions are made approximately 50 ns after a CLK edge until conversion is complete. At the end of conversion, the $\overline{INT}$ line goes low 100 ns (typically) after the LSB decision and the SAR contents are transferred to the output latch. The SAR is then reset in readiness for a new conversion.

Track-and-Hold

The track-and-hold (T/H) amplifier on the analog input to the ADC of the AD7769 allows the ADC to accurately convert an input sine wave of 5 V peak-to-peak amplitude up to a frequency of 200 kHz, the Nyquist frequency of the ADC when operated at its maximum throughput rate of 400 kHz. This maximum rate of conversion includes conversion time and time between conversions. Because the input bandwidth of the track-and-hold is much greater than 200 kHz, the input signal should be band limited to avoid folding unwanted signals into the band of interest.

DAC Outputs

The D/A converter outputs are buffered with on-board, high speed op amps that are capable of driving 5 kΩ and 100 pF loads to AGND (DAC). Each output amplifier settles to within 1/2 LSB of its final output value in typically less than 2.5 µs. See Figures 9 and 10 for waveforms of the typical output settling time performance.

The output noise from the amplifiers with full scale on the DACs is typically 200 µV peak-to-peak.

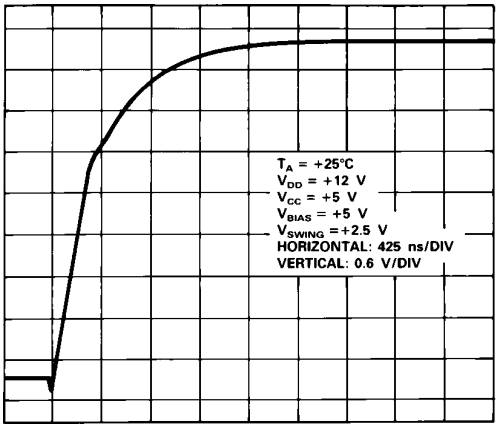


Figure 9. Positive-Going Settling Time

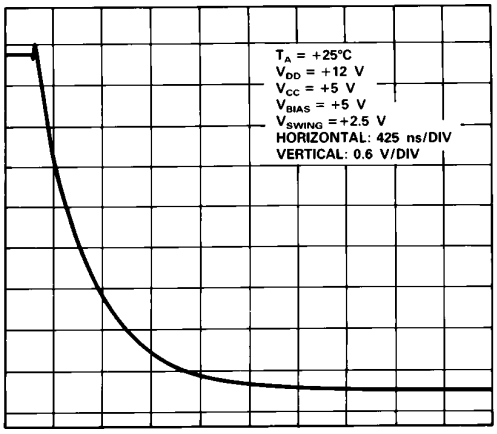


Figure 10. Negative-Going Settling Time

Internal / External Clock Operation

The AD7769 can be operated on either its own internal clock or with an externally applied clock signal. For internal clock operation the CLK input must be tied to V_{DD}. No external components are required. The internal clock typically runs at 5 MHz giving a typical conversion time of 2.5 µs. For external clock operation the CLK input must be driven with a TTL/ HCMOS compatible input. The mark/space ratio of the clock signal can vary from 30/70 to 70/30. For an input frequency of 5 MHz, the conversion time is 2.5 µs.

Digital Inputs and Outputs

The AD7769 communicates over a standard, 8-bit microprocessor data bus and is controlled by standard mpu control lines, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{INT}$, plus two address lines, $\overline{ADC}$/DAC and $\overline{CHA}$/CHB, which select the DAC or ADC function and Channel A or Channel B input/output channel. The Chip Select ($\overline{CS}$) line selects the device, Write ($\overline{WR}$) is used to initiate ADC conversions or to write data to the DAC, depending on the state of $\overline{ADC}$/DAC. $\overline{INT}$ is a status flag that indicates completion of a conversion, while $\overline{RD}$ is used to read ADC output data. The 8-bit data port (DB0–DB7) is a bidirectional port into which data can be written to the two DAC registers, and from which data can be read from the ADC register. ADC output data may also be written directly into either of the DAC registers.

These logical operations are detailed in Table I and in the time ing diagrams, Figures 11 to 13. Figures 12 and 13 show the fairly straightforward operations of reading ADC data and writing data to the DACs, and need little explanation. Figure 11 shows the timing for ADC channel selection and conversion start. This is more complicated as the state of the data outputs during a conversion depends on $\overline{CS}$ and $\overline{RD}$.

To initiate a conversion (or any other operation) the device must be selected by taking $\overline{CS}$ low. A conversion is started by taking $\overline{WR}$ low, then high again (conversion starts on rising edge of $\overline{WR}$). There are three possibilities for the state of the data outputs during the conversion.

1. If $\overline{RD}$ is held high, the data outputs will be high impedance throughout the conversion.
2. If $\overline{RD}$ and $\overline{CS}$ are both held low until after $\overline{INT}$ goes low, then DB0–DB7 will initially output data from the last conversion. After $\overline{INT}$ goes low the new conversion data will appear on DB0–DB7.

OBSOLETE

3. If $\overline{RD}$ is held low but $\overline{CS}$ is taken high during the conversion, the device will be de-selected and DB0–DB7 will revert to their high impedance state. This will not affect completion of the conversion, but the data cannot be read, or any other operation performed, until $\overline{CS}$ is taken low again.
4. Note that the state of $\overline{RD}$ should not be changed during a conversion.

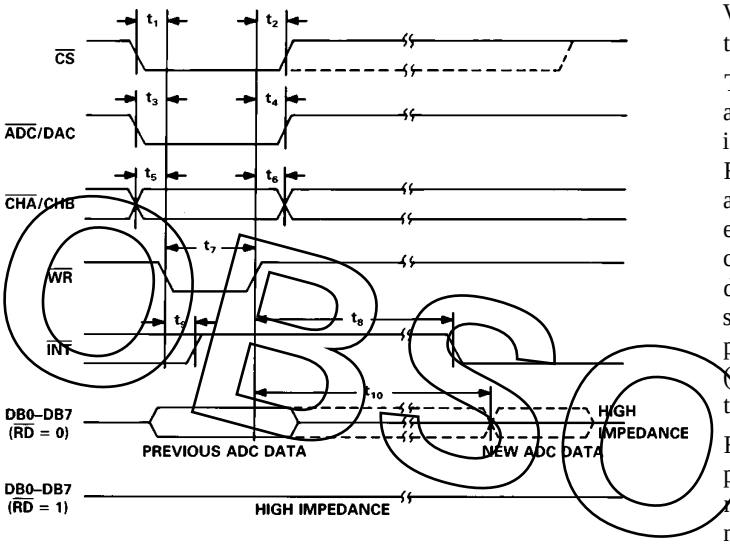


Figure 11. Timing for ADC Channel Select and Conversion Start

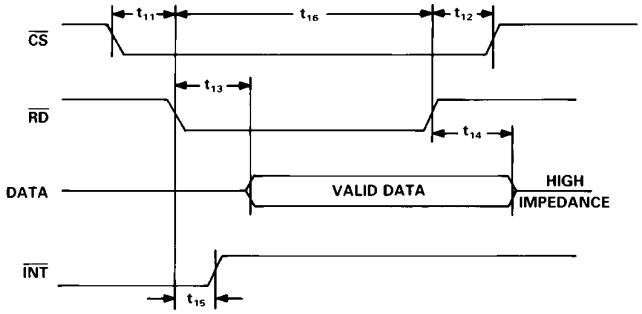
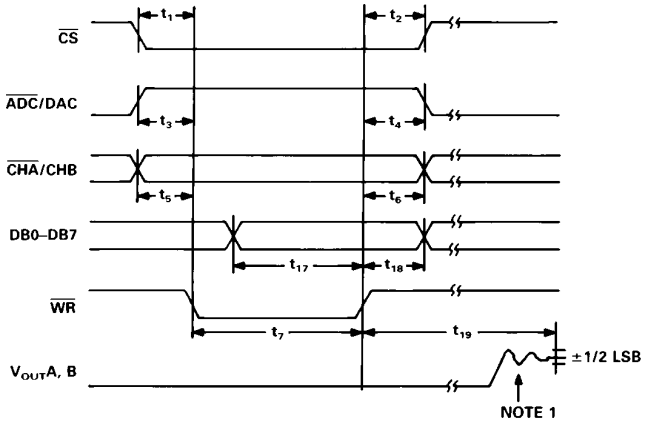


Figure 12. Timing for ADC Data Read



NOTE 1. THE TIME AXIS IS COMPRESSED FOR THIS SECTION OF THE DIAGRAM

Figure 13. Timing for DAC Channel Select and Data Write

DIGITAL SIGNAL PROCESSING APPLICATIONS

In Digital Signal Processing (DSP) application areas like voice recognition, echo cancellation and adaptive filtering, the dynamic characteristics (SNR, Harmonic Distortion, Intermodulation Distortion) of both the ADC and DACs are critical. The AD7769 is specified dynamically as well as with standard dc specifications. Because the track/hold amplifier has a wide bandwidth, an antialiasing filter should be placed on the $V_{IN}A$ and $V_{IN}B$ inputs to avoid aliasing of high frequency noise back into the bands of interest.

The dynamic performance of the ADC is evaluated by applying a sine wave signal of very low distortion to the $V_{IN}A$ or $V_{IN}B$ input which is sampled at a 409.6 kHz sampling rate. A Fast Fourier Transform (FFT) plot or Histogram plot is then generated from which SNR, harmonic distortion and dynamic differential nonlinearity data can be obtained. For the DACs, the codes for an ideal sine wave are stored in PROM and loaded down to the DAC. The output spectrum is analyzed, using a spectrum analyzer to evaluate SNR and harmonic distortion performance. Similarly, for intermodulation distortion, an input (either to VIN or DAC code) consisting of pure sine waves at two frequencies is applied to the AD7769.

Figure 14 shows a 2048 point FFT plot of the ADC with an input signal of 130 kHz. The SNR is 49.2 dB. It can be seen that most of the harmonics are buried in the noise floor. It should be noted that the harmonics are taken into account when calculating the SNR. The relationship between SNR and resolution (N) is expressed by the following equation:

$$SNR = (6.02N + 1.76)\,dB$$

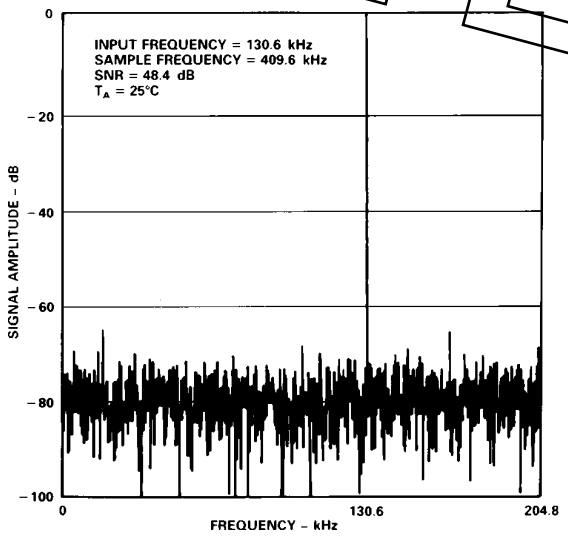


Figure 14. ADC FFT Plot

OBSOLETE

This is for an ideal part with no differential or integral linearity errors. These errors will cause a degradation in SNR. By working backwards from the above equation, it is possible to get a measure of ADC performance expressed in effective number of bits (N). The effective number of bits is plotted versus frequency in Figure 15. The effective number of bits typically falls between 7.7 and 7.9, corresponding to SNR Figures 48.1 and 49.7 dB.

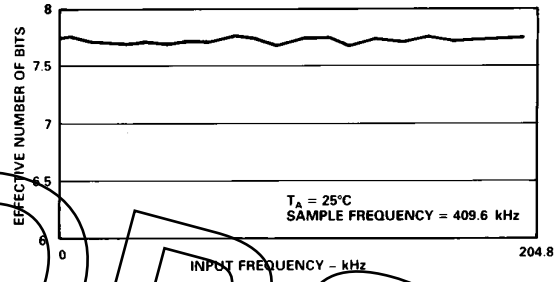


Figure 15. Effective Number of Bits vs. Frequency

Figure 16 shows a spectrum analyzer plot of the output spectrum from one of the DACs with an ideal sine wave table loaded to the data inputs of the DAC. In this case, the SNR is 47 dB.

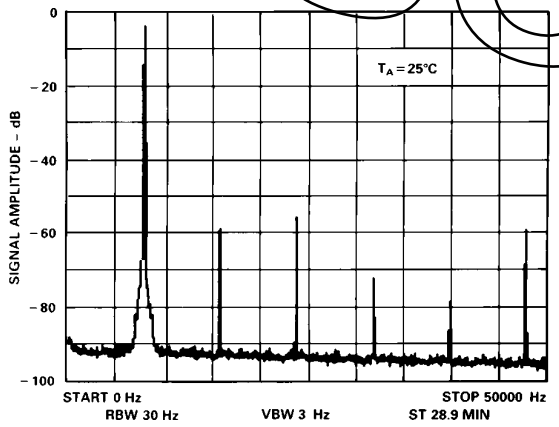


Figure 16. DAC Output Spectrum

Histogram Plot

When a sine wave of specified frequency is applied to the $V_{IN}A$ or $V_{IN}B$ input of the AD7769 and several thousand samples are taken, it is possible to plot a histogram showing the frequency of occurrence of each of the 256 ADC codes. If a particular step is wider than the ideal 1 LSB width, then the code associated with that step will accumulate more counts than for the code for an ideal step. Likewise, a step narrower than ideal width will have fewer counts. Missing codes are easily seen because a missing code means zero counts for a particular code. The absence of large spikes in the plot indicates small differential nonlinearity.

Figure 17 shows a histogram plot for the ADC indicating very small differential nonlinearity and no missing codes for an input frequency of 204 kHz. For a sine wave input, a perfect ADC would produce a probability density function described by the equation:

$$p\,(V) = \frac{1}{\pi(A^2 - V^2)^{1/2}}$$

where A is the peak amplitude of the sine wave and $p\,(V)$ the probability of occurrence at a voltage V. The histogram plot of Figure 17 corresponds very well with this shape.

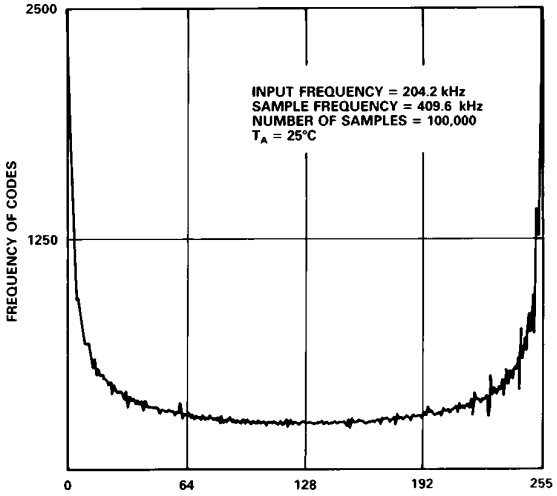


Figure 17. ADC Histogram Plot

In digital signal processing applications, where the AD7769 is used to sample ac signals, it is essential that the signal sampling occurs at exactly equal intervals. This minimizes errors due to sampling uncertainty or jitter. A precise timer or clock source, to start the conversion process, is the best method of generating equidistant sampling intervals.

MICROPROCESSOR / MICROCOMPUTER INTERFACING

The AD7769 is designed for easy interfacing to microprocessors and microcomputers as a memory mapped peripheral or an I/O device. In addition, the AD7769 high speed bus timing allows direct interfacing to many DSP processors such as the TMS320C10 and ADSP-2101.

AD7769–TMS320C10 Interface

A typical interface to the TMS320C10 is shown in Figure 18. The AD7769 is mapped at a port address, and the interface is designed for the maximum TMS320C10 clock frequency of 20 MHz.

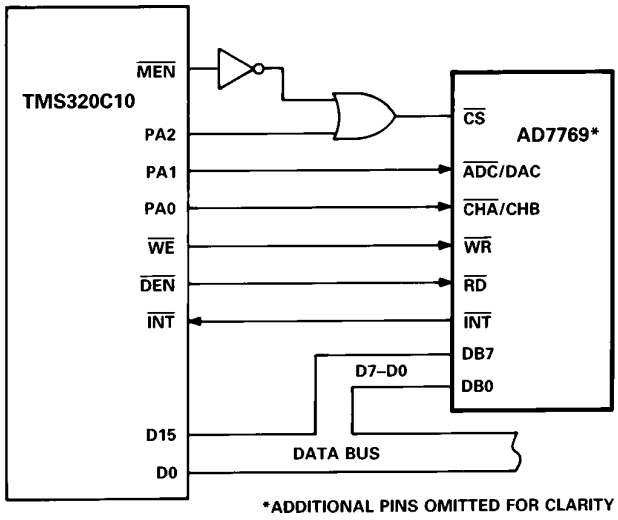


Figure 18. AD7769 to TMS320C10 Interface

OBSOLETE

Conversion is initiated on the selected AD7769 ADC channel using a single I/O instruction, <OUT ADC, A>. The processor then polls $\overline{INT}$ until it goes low before reading the conversion result using an <IN A, ADC> instruction. Writing data to the relevant AD7769 DAC consists of an <OUT DAC, A> instruction.

AD7769–ADSP-2101 Interface

Figure 19 shows a typical interface to the DSP microcomputer, the ADSP-2101. The ADSP-2101 is optimized for high speed numeric processing tasks.

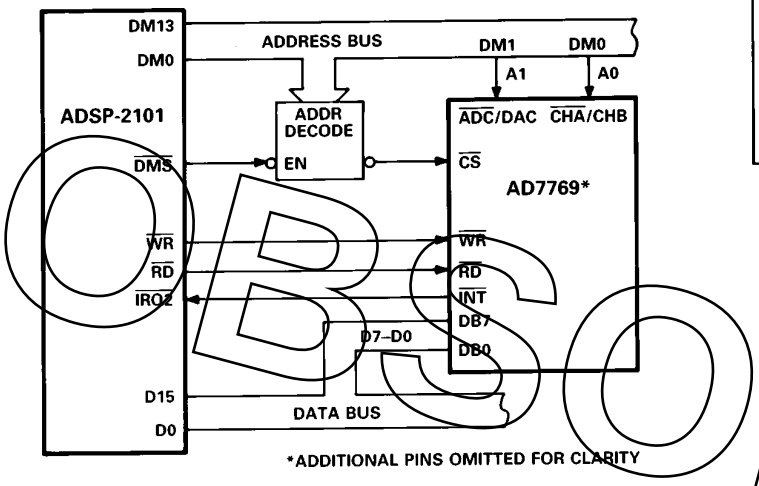


Figure 19. AD7769 to ADSP-2101 Interface

Because the instruction cycle of the ADSP-2101 is very fast (80 ns cycle), the $\overline{WR}$ and $\overline{RD}$ pulses must be stretched out to suit the AD7769. This is easily achieved as the ADSP-2101 memory interface supports slower memories and memory-mapped peripherals (i.e., AD7769) with a programmable wait state generation capability. A number of wait states, from 0 to 7, can be specified for each memory interface. One wait state is sufficient for the interface to the AD7769.

AD7769–8051 Interface

A choice of two interface modes are available to the 8051 microcomputer.

Figure 20 shows a typical interface to the 8051 processor bus. It is suitable for the maximum 8051 clock frequency of 12 MHz. In this interface mode, Port 0 provides the multiplexed low order address and data bus and Port 2 provides the high order address bus (A_8–A_{15}).

Figure 21 shows the AD7769 interfaced to the 8051 parallel I/O ports. This interface circuit is simpler to implement than the previous interface to the processor bus, but, in general, the maximum data throughput rate is much slower (for the same clock frequencies). In addition to its simplicity, the interface to the parallel I/O ports versus the processor bus allows independent control of both the $\overline{WR}$ and $\overline{RD}$ inputs to the AD7769.

For example, the 8051 can set both $\overline{WR}$ and $\overline{RD}$ low at the same time. This permits data from the last ADC conversion to be written directly from the ADC register into the selected DAC register (see Logic Truth Table). This allows very fast transfer of data from the ADC to the DAC and is a useful feature for some applications such as a fast, programmable, infinite sample-and-hold function.

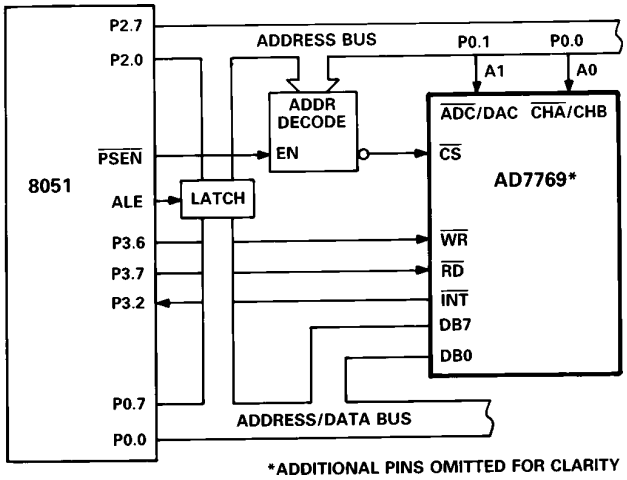


Figure 20. AD7769 to 8051 (Processor Bus) Interface

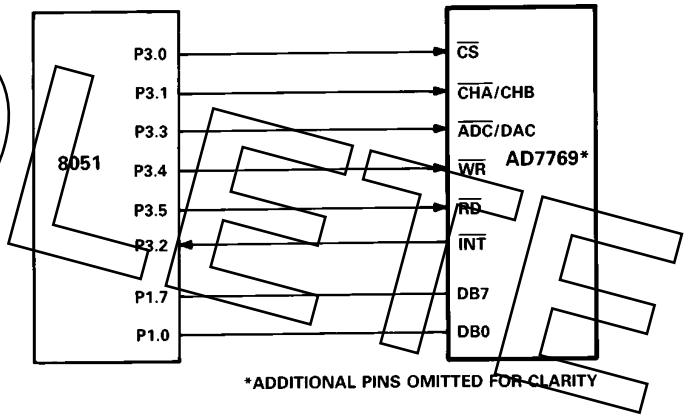


Figure 21. AD7769 to 8057 (Parallel I/O Ports) Interface

AD7769–MC68HC11 Interface

Figure 22 shows a typical interface between the AD7769 and the MC68HC11 microcomputer. This interface is designed for the maximum MC68HC11 clock speed of 8.4 MHz. The microcomputer is operated in the expanded multiplexed mode, with the AD7769 as a memory mapped peripheral. The expansion bus is made up of Ports B and C, and control signals AS and R/$\overline{W}$.

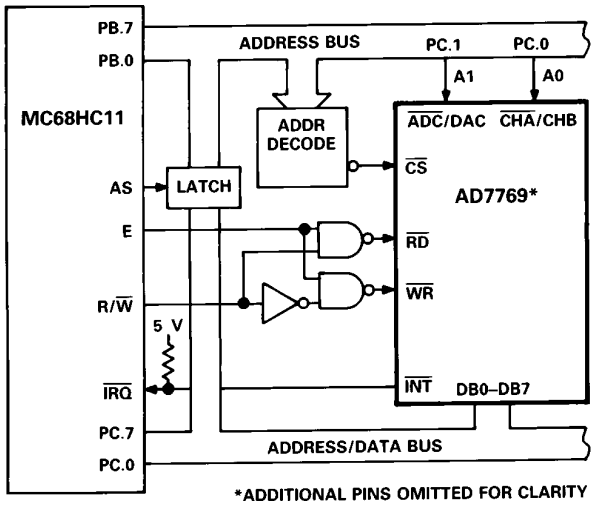


Figure 22. AD7769 to MC68HC11 Interfaced

APPLICATIONS

The AD7769 analog I/O port is used to convert servo related signals between the analog and digital domains. The input structure of the two-channel ADC makes it very easy to convert the typical output signals provided by a servo demodulator.

In a magnetic disk drive employing a dedicated servo surface, the servo demodulator produces two, positive-only, quadrature signals, generally sinusoidal or triangular, from the all-bit patterns read from the servo surface. The quadrature signals have the form of $V_{BIAS} \pm V_{SWING}$. The very fast conversion time of the AD7769 ADC allows sequential conversion of these quadrature signals without introducing significant phase delay errors. These converted signals provide the servo microcontroller with position and track crossing information from which velocity information can be derived. In optical disk drives, analogous servo signals can be derived from the quad photodiode detector to provide position and focus information for the microcontroller.

The two DACs in the AD7769 accept servo data from the microcontroller to position the head assembly. The DACs provide positive-only output signals of the form $V_{BIAS} \pm V_{SWING}$, which are ideal for driving voice coil motors. In magnetic disk drives, a single voice coil motor is used to position the head assembly and one DAC is usually sufficient to drive the motor in both the seek and track modes. In the seek mode, the DAC can be used to generate directly the desired analog velocity trajectory which the head must travel in order to achieve minimum access times. Alternatively, the DAC can generate a servo error value (computed by the microcontroller) between the actual head velocity and the desired head velocity. In the track mode, the DAC can be used to provide a position error signal to keep the head over the track or to detent the head off track, for such purposes as thermal compensation and soft error retries. The second DAC in the AD7769 may be employed in this fine positioning loop. Alternatively, the second DAC can be used to control the speed of the spindle motor via a pulse width modulator. In optical disk drives two voice coil motors are used, requiring both DACs of the AD7769–one for the focus servo loop and one for the radial positioning servo loop.

A typical servo control loop using the AD7769 is shown in Figure 23. In this dedicated servo drive, the servo demodulator converts the servo information bit patterns from the disk into the standard N and Q (normal and quadrature) servo signals. The voice coil motor current, I_L, is bidirectional and is supplied by the power transconductance amplifier. One input to this amplifier is held at V_{BIAS} (DAC), while the other input is driven from a DAC output, V_{OUT} A/B. Typical input/output waveforms for this power stage are shown in Figure 24. The transconductance, G_O, of the power stage is determined by external sense resistors.

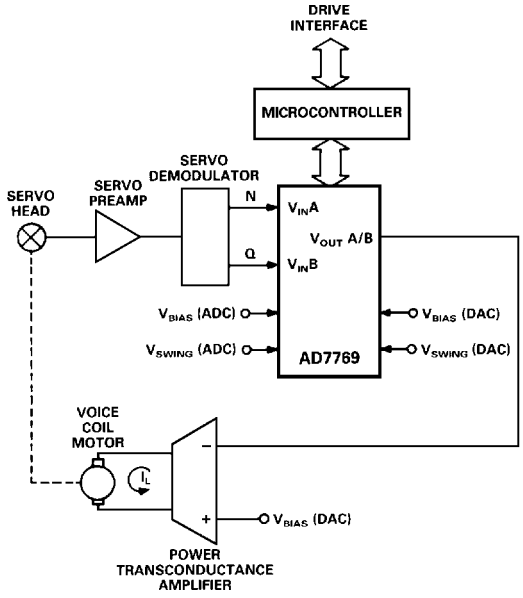


Figure 23. Typical Dedicated Servo Control Loop Using the AD7769

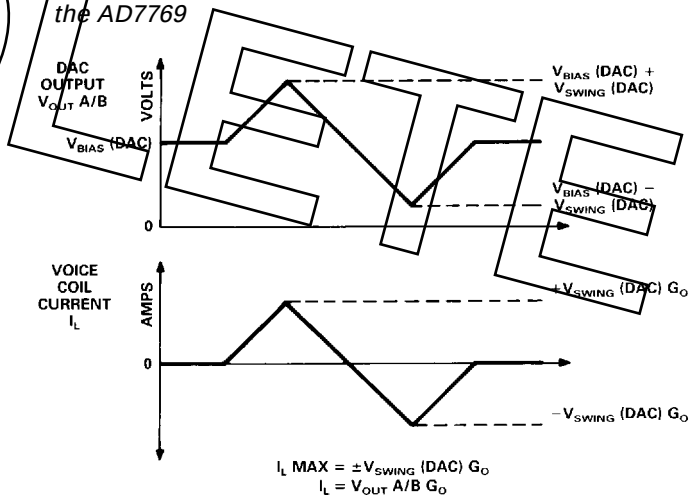


Figure 24. Typical Relationship Between Input Voltage and Output Current for Transconductance Amplifier

Increased Resolution DAC Output

Since both V_{BIAS} (DAC) and V_{SWING} (DAC) are common to both output channels, the full-scale output voltages of both channels are nominally identical. However, by adding an external op amp and scaling resistors, it is possible to attenuate the full-scale output voltage of one (or both) of the DAC outputs to effectively increase the output voltage resolution. Figure 25 shows channel A being attenuated using a resistor scaling of 10:1. The attenuated output voltage, $V_{OUT}A'$, is

$$V_{OUT}A' = V_{BIAS} + (V_{SWING}/10)(2D_A - 1).$$

The output voltage of Channel B remains at

$$V_{OUT}B = V_{BIAS} + V_{SWING}\,(2D_B - 1).$$

D_A and D_B are fractional representations of the DAC input codes, e.g., $D_A = N_A/256$ and $D_B = N_B/256$. For example, with a V_{SWING} voltage level of 2 V, the Channel B output span is 4 V with an LSB size of 15.6 mV and (attenuated) Channel A output span is 400 mV with an LSB size of 1.56 mV. Changing the resistor scaling in Figure 25 obviously changes the attenuated full-scale output.

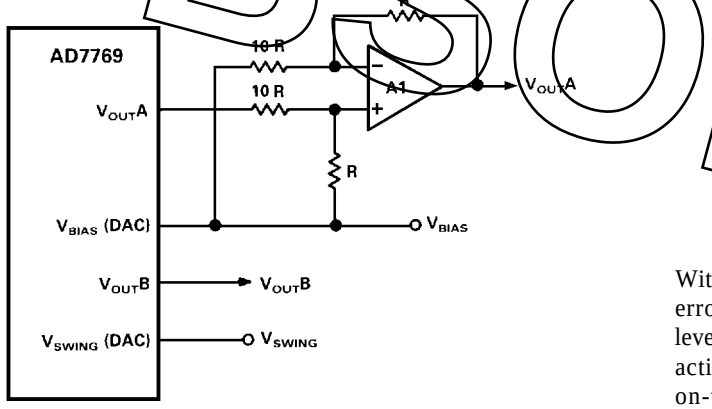


Figure 25. Increasing the DAC Output Voltage Resolution

A single change to the circuit Figure 25 allows the two DAC outputs to be combined to provide a single analog output with resolution beyond the standard 8-bits. Figure 26 shows the rearranged circuit. The composite output, V_{OUT}, is

$$V_{OUT} = V_{OUT}B + (V_{SWING}/10)(2D_A - 1)$$

or

$$V_{OUT} = V_{BIAS} + V_{SWING}\,(2D_B - 1) + (V_{SWING}/10)\,(2D_A - 1).$$

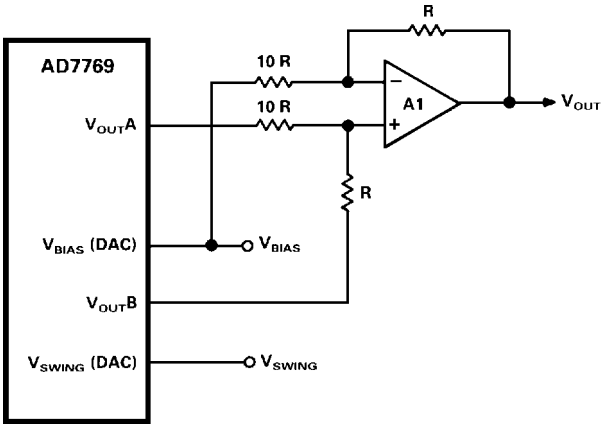


Figure 26. Combined $V_{OUT}A$, $V_{OUT}B$ Circuit

DAC A can be programmed to produce an interpolation function between the 8-bit steps of DAC B to allow, for example, very smooth velocity profile waveforms to be generated.

Servo Offset Facility

Most dedicated servo disk drives offer an offset facility whereby some small voltage is injected into the track-following loop. The purpose of the offset is to move the head to the right or left of its current on-track position to permit reading of off-track data. The circuit is shown in Figure 27. With the 10:1 resistor scaling used in the circuit the output voltage, V_{OUT}, is

$$V_{OUT} = V_{PE} + (V_{SWING}/10)\,(2D_A - 1).$$

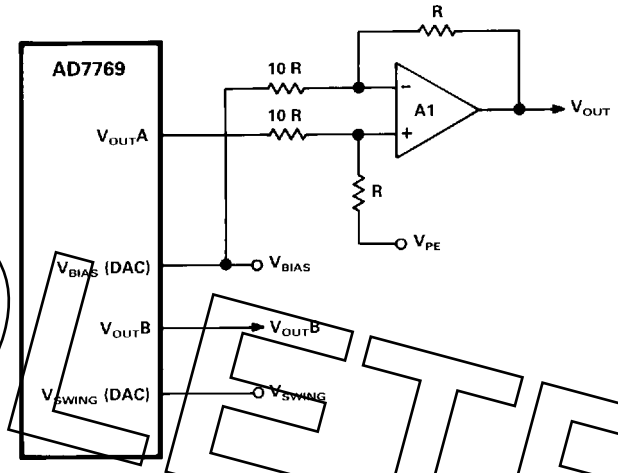


Figure 27. Servo Offset Facility

With no offset added, $V_{OUT} = V_{PE}$, where V_{PE} is the position error voltage which the servo loop normally drives to its zero level, V_{BIAS}. When an offset voltage is supplied by DAC A, the action of the servo is to move the head away from its current on-track position until the position error voltage is equal and opposite to the offset voltage. The position of the head about the track centre is thus programmable.

Programmable Full-Scale Range

The output voltage span of both DACs is determined by the V_{SWING} (DAC) voltage level. This is normally supplied from some fixed voltage source. However, it is possible to use one of the DAC channels to generate a programmable V_{SWING} voltage level. The remaining channel will thus have a full-scale range and LSB size which is software programmable. This circuit is shown in Figure 28 where $V_{OUT}B$ is used in an implicit feedback loop to generate a programmable swing voltage, V_{SWING} (DAC), for the AD7769 from an external fixed input swing voltage, V_{SWING}. Using the 5:1 resistor scaling shown in Figure 28, the expression for the AD7669 input swing voltage is

$$V_{SWING}\,(DAC) = \frac{V_{SWING}}{1 - \frac{(2D_B - 1)}{5}}.$$

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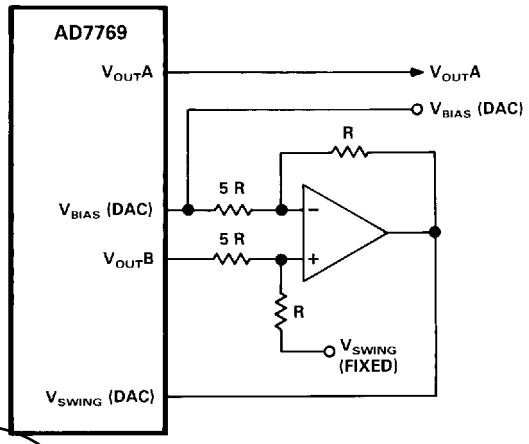

Figure 28. Generating a Software Programmable V_{SWING} (DAC)

For example, with a fixed input swing voltage of 2.5 V, the programmable span via DAC B is as follows:

$D_B = 0$: V_{SWING} (DAC) = 2.08

$D_B = 1/2$: V_{SWING} (DAC) = 2.5 V = V_{SWING}

$D_B \approx 1$: V_{SWING} (DAC) = 3.125 V

The AD7769 is specified for a V_{SWING} (DAC) voltage range from 2 V to 3 V, although in practice this range can be extended while still maintaining monotonic operation.

Closed Loop Microstepping

Microstepping is a popular technique in low density disk drives (both floppy and hard disk) which allows higher positional resolution of the disk drive head over that obtainable from a full-step driven stepper motor. Typically, a two-phase stepper motor has its phase currents driven with a sine-cosine relationship. These cosinusoidal signals are generated by two DACs driven with the appropriate data. The resolution of the DACs determines the number of microsteps into which each full step can be divided. For example, with a 1.8° full-step motor and a 4-bit DAC, a microstep size of 0.11° (1.8°/2^n) is obtainable.

The microstepping technique improves the positioning resolution possible in any control application. However, the positional accuracy can be significantly worse than that offered by the original full-step accuracy specification due to load torque effects. To ensure that the increased resolution is useable, it is therefore necessary to use a closed-loop system where the position of the disk drive head (or motor) is monitored. The closed-loop system allows an error between the desired position and the actual position to be monitored and corrected. The correction is achieved by adjusting the ratio of the phase currents in the motor windings until the required head position is reached.

The AD7769 is ideally suited for the closed-loop microstepping technique with its dual DACs for positioning the disk drive head and dual channel ADC for monitoring the position of the head. A typical circuit for a closed-loop microstepping system is shown in Figure 29. The DAC waveforms are shown in Figure 30 along with the direction information of clockwise rotation supplied by the controller.

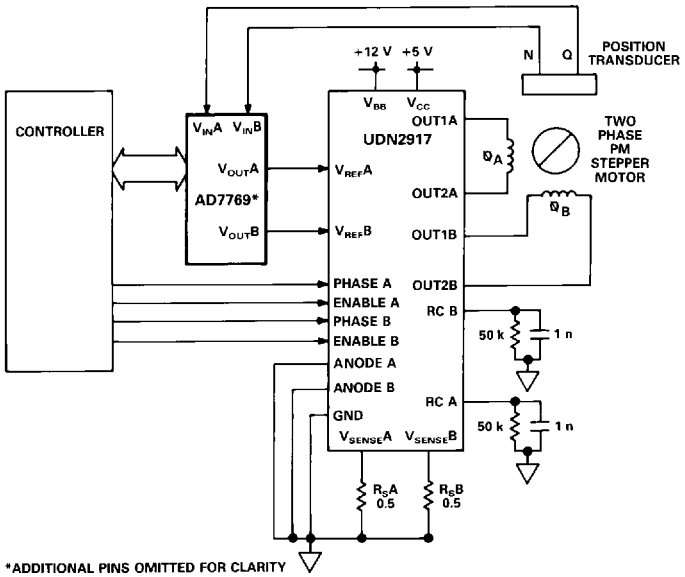

Figure 29. Typical Closed-Loop Microstepping Circuit with the AD7769

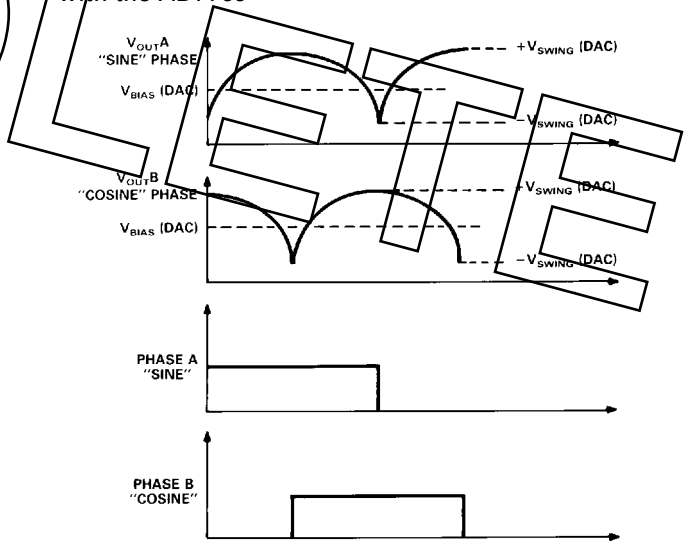

Figure 30. Typical Control Waveforms for the Microstepping Circuit of Figure 29

A typical transducer would be a moire-fringe transducer which consists of two gratings, one fixed and one moveable. The relative positions of these two gratings will modulate the amount of light from a LED which can pass through. In order to derive head direction information the stationary grating has two sets of bars, with a 90° phase relationship, and two photo-transistors. The quadrature sinusoidal output waveforms (N & Q) can be converted directly by the AD7769.

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Multichannel Expansion

In some applications, more than two analog input channels are required to be converted by the ADC. Figure 31 shows a circuit configuration for such an application. The ADG528A is a latched, B-channel analog multiplexer that is ideally suited for this application since it is specified for single supply operation (+12 V ±10%).

The $\overline{CS}$, $\overline{ADC}$/DAC and $\overline{WR}$ inputs of the AD7769 are gated to drive the $\overline{WR}$ input of the ADG528A. The multiplexer input signal is selected on the falling edge of the $\overline{WR}$ pulse while the signal is latched on the rising edge. Also, on the rising edge of $\overline{WR}$, the AD7769 ADC starts conversion. Therefore, the output signal of the multiplexer must have settled to within 8-bits over the duration of the $\overline{WR}$ pulse (see ADC Conversion Cycle section for details). The t_{ON} ($\overline{WR}$) and settling time of the ADG528A thus determines the width of the $\overline{WR}$ pulse.

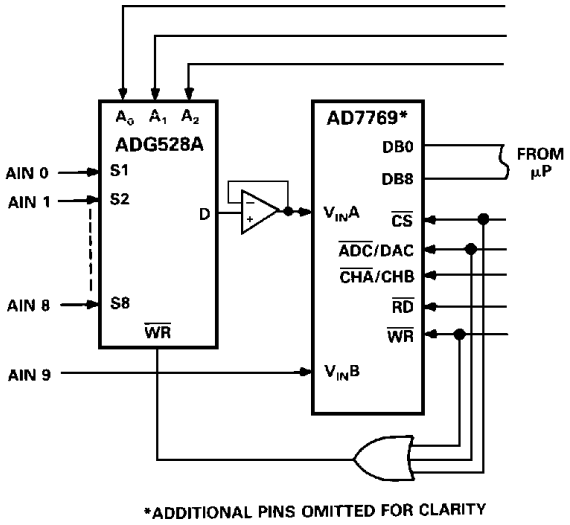

Figure 31. Multichannel Inputs

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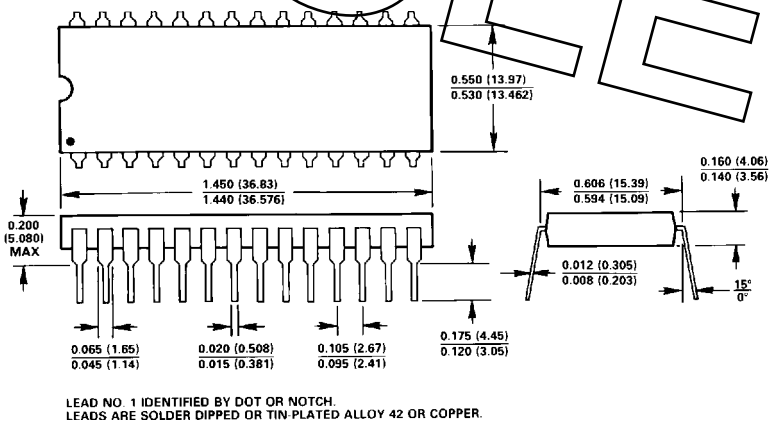
OUTLINE DIMENSIONS

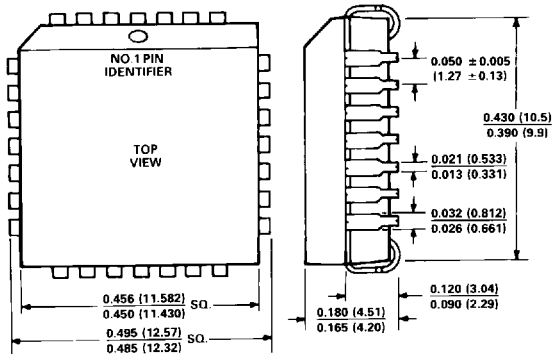
Dimensions shown in inches and (mm).

28-Pin Plastic DIP (N-28)



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
LEADS ARE SOLDER DIPPED OR TIN-PLATED ALLOY 42 OR COPPER.

28-Terminal Plastic Leaded Chip Carrier (P-28A)



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