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FAIRCHILD SEMICONDUCTOR®

October 2011

FSQ0170RNA, FSQ0270RNA
Green Mode Fairchild Power Switch (FPS™)

Features

- Internal Avalanche Rugged 700V SenseFET
- Consumes only 0.8W at 230 V_{AC} & 0.5W Load with Burst-Mode Operation
- Precision Fixed Operating Frequency, 100kHz
- Internal Start-up Circuit and Built-in Soft-Start
- Pulse-by-Pulse Current Limiting and Auto-Restart Mode
- Over-Voltage Protection (OVP), Overload Protection (OLP), Internal Thermal Shutdown Function (TSD)
- Under-Voltage Lockout (UVLO)
- Low Operating Current (3mA)
- Adjustable Peak Current Limit

Applications

- Auxiliary Power Supply for PC and Server
- SMPS for VCR, SVR, STB, DVD & DVCD Player, Printer, Facsimile & Scanner
- Adapter for Camcorder

Related Application Notes

- *AN-4134: Design Guidelines for Off-line Forward Converters Using Fairchild Power Switch (FPS™)*
- *AN-4137: Design Guidelines for Off-line Flyback Converters Using Fairchild Power Switch (FPS™)*
- *AN-4141: Troubleshooting and Design Tips for Fairchild Power Switch (FPS™) Flyback Applications*
- *AN-4147: Design Guidelines for RCD Snubber of Flyback*
- *AN-4148: Audible Noise Reduction Techniques for FPS™ Applications*

Description

The FSQ0170RNA, and FSQ0270RNA, consists of an integrated current mode Pulse Width Modulator (PWM) and an avalanche-rugged 700V Sense FET. It is specifically designed for high-performance off-line Switch Mode Power Supplies (SMPS) with minimal external components. The integrated PWM controller features include: a fixed-frequency generating oscillator, Under-Voltage Lockout (UVLO) protection, Leading Edge Blanking (LEB), an optimized gate turn-on/turn-off driver, Thermal Shutdown (TSD) protection, and temperature compensated precision current sources for loop compensation and fault protection circuitry.

Compared to a discrete MOSFET and controller or RCC switching converter solution, the FSQ0170RNA, and FSQ0270RNA reduces total component count, design size, and weight while increasing efficiency, productivity, and system reliability. These devices provide a basic platform that is well suited for the design of cost-effective flyback converters, as in PC auxiliary power supplies.

8-DIP

Ordering Information

Product Number	Package	Marking Code	BV_{DSS}	f_{OSC}	$R_{DS(ON)\ (MAX.)}$
FSQ0170RNA	8DIP	Q0170RA	700V	100kHz	11Ω
FSQ0270RNA	8DIP	Q0270RA	700V	100kHz	7.2Ω

FPS™ is a trademark of Fairchild Semiconductor Corporation.

Application Diagram

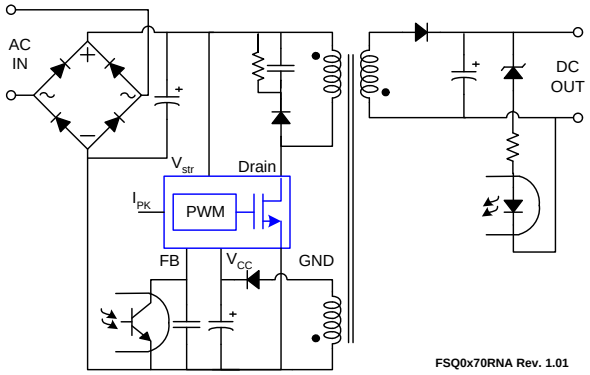


Figure 1. Typical Flyback Application

Output Power Table(1)

Product	230V$_{AC}$ ±15%(2)		85–265V$_{AC}$	
	Adapter(3)	Open Frame(4)	Adapter(3)	Open Frame(4)
FSQ0170RNA	14W	20W	9W	13W
FSQ0270RNA	17W	24W	11W	16W

Notes:

1. The maximum output power can be limited by junction temperature.
2. 230 V_{AC} or 100/115 V_{AC} with doubler.
3. Typical continuous power in a non-ventilated enclosed adapter with sufficient drain pattern as a heat sink, at 50°C ambient.
4. Maximum practical continuous power in an open-frame design with sufficient drain pattern as a heat sink, at 50°C ambient.

Internal Block Diagram

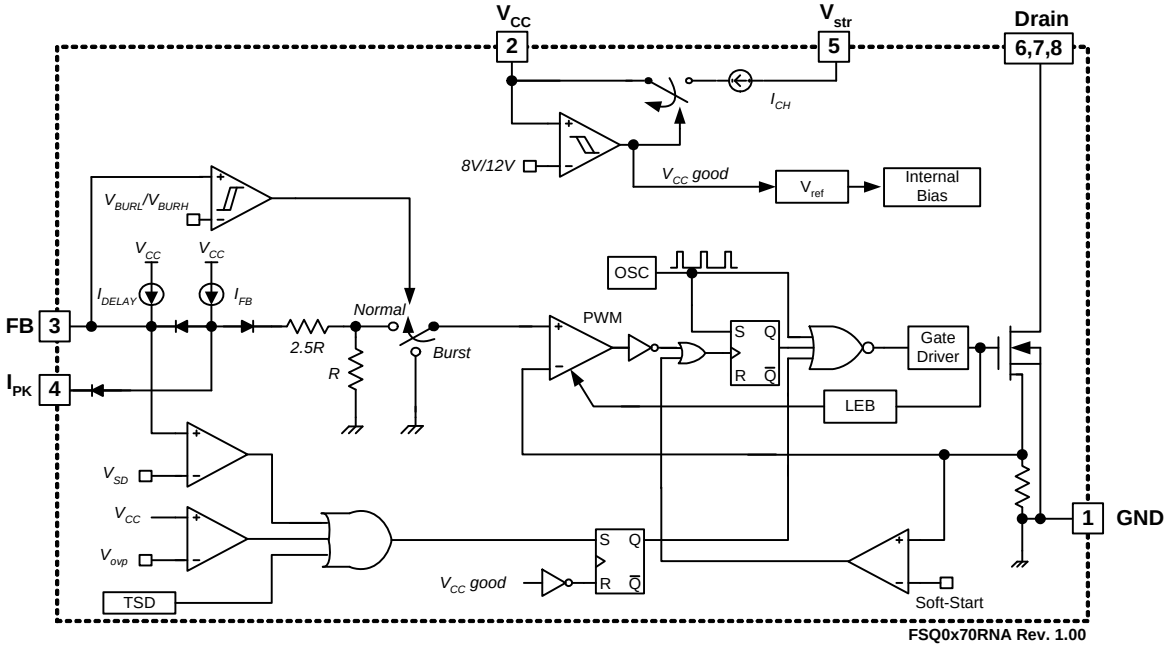


Figure 2. Internal Block Diagram

Pin Configuration

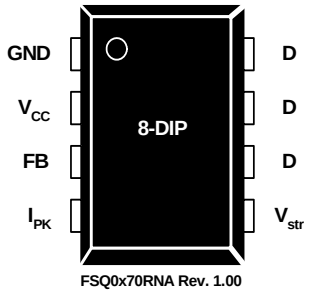


Figure 3. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	GND	**Ground.** SenseFET source terminal on primary side and internal control ground.
2	V_{CC}	**Power Supply.** Positive supply voltage input. Although connected to an auxiliary transformer winding, current is supplied from pin 5 (V_{str}) via an internal switch during start-up, see Figure 2. It is not until V_{CC} reaches the UVLO upper threshold (12V) that the internal start-up switch opens and device power is supplied via the auxiliary transformer winding.
3	FB	**Feedback.** The feedback voltage pin is the non-inverting input to the PWM comparator. It has a 0.9mA current source connected internally while a capacitor and opto-coupler are typically connected externally. A feedback voltage of 6V triggers overload protection (OLP). There is a time delay while charging external capacitor C_{FB} from 3V to 6V using an internal 5μA current source. This time delay prevents false triggering under transient conditions, but still allows the protection mechanism to operate under true overload conditions.
4	I_{PK}	**Peak Current Limit.** This pin adjusts the peak current limit of the SenseFET. The 0.9mA feedback current source is diverted to the parallel combination of an internal 2.8kΩ resistor and any external resistor to GND on this pin. This determines the peak current limit. If this pin is tied to V_{CC} or left floating, the typical peak current limit is 0.8A (FSQ0170RNA), 0.9A (FSQ0270RNA).
5	V_{str}	**Start-up.** This pin connects to the rectified AC line voltage source. At start-up, the internal switch supplies internal bias and charges an external storage capacitor placed between the V_{CC} pin and ground. Once the V_{CC} reaches 12V, the internal switch is opened.
6	Drain	**SenseFET drain.** High-voltage power SenseFET drain connection.
7	Drain	**SenseFET drain.** High-voltage power SenseFET drain connection.
8	Drain	**SenseFET drain.** High-voltage power SenseFET drain connection.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only

Symbol	Characteristic		Value	Unit
V_{DRAIN}	Drain Pin Voltage		700	V
V_{STR}	Vstr Pin Voltage		700	V
I_{DM}	Drain Current Pulsed[5]	FSQ0170RNA	4	A
		FSQ0270RNA	8	
E_{AS}	Single Pulsed Avalanche Energy[6]	FSQ0170RNA	50	mJ
		FSQ0270RNA	140	
V_{CC}	Supply Voltage		20	V
V_{FB}	Feedback Voltage Range		-0.3 to V_{CC}	V
P_D	Total Power Dissipation		1.5	W
T_J	Operating Junction Temperature		Internally limited	°C
T_A	Operating Ambient Temperature		-25 to +85	°C
T_{STG}	Storage Temperature		-55 to +150	°C

Notes:

5. Non-repetitive rating: Pulse width is limited by maximum junction temperature.
6. L = 51mH, starting T_J = 25°C.

Thermal Impedance

T_A = 25°C, unless otherwise specified. All items are tested with the standards JESD 51-2 and 51-10 (DIP).

Symbol	Parameter	Value	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance[7]	80	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance[8]	20	°C/W
θ_{JT}	Junction-to-Top Thermal Resistance[9]	35	°C/W

Notes:

7. Free standing with no heatsink; without copper clad.
   (Measurement Condition - Just before junction temperature T_J enters into OTP.)
8. Measured on the DRAIN pin close to plastic interface.
9. Measured on the PKG top surface.

Electrical Characteristics

T_A = 25°C unless otherwise specified.

Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit
SenseFET Section[10]							
I_{DSS}	Zero-Gate-Voltage Drain Current		V_{DS} = 700V, V_{GS} = 0V			50	μA
			V_{DS} = 560V, V_{GS} = 0V, T_C = 125°C			200	
$R_{DS(ON)}$	Drain-Source On-State Resistance[11]	FSQ0170RNA	V_{GS} = 10V, I_D = 0.5A		8.8	11	Ω
		FSQ0270RNA			6.0	7.2	
C_{ISS}	Input Capacitance	FSQ0170RNA	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		250		pF
		FSQ0270RNA			550		
C_{OSS}	Output Capacitance	FSQ0170RNA			25		
		FSQ0270RNA			38		
C_{RSS}	Reverse Transfer Capacitance	FSQ0170RNA			10		
		FSQ0270RNA			17		
$t_{d(on)}$	Turn-On Delay Time	FSQ0170RNA	V_{DS} = 350V, I_D = 1.0A		12		ns
		FSQ0270RNA			20		
t_r	Rise Time	FSQ0170RNA			4		
		FSQ0270RNA			15		
$t_{d(off)}$	Turn-Off Delay Time	FSQ0170RNA			30		
		FSQ0270RNA			55		
t_f	Fall Time	FSQ0170RNA			10		
		FSQ0270RNA			25		
Control Section							
f_{OSC}	Switching Frequency			92	100	108	KHz
Δf_{OSC}	Switching Frequency Variation[10]		-25°C ≤ T_A ≤ 85°C		±5	±10	%
D_{MAX}	Maximum Duty Cycle		Measured at 0.1 x V_{DS}	55	60	65	%
D_{MIN}	Minimum Duty Cycle			0	0	0	%
V_{START}	UVLO Threshold Voltage		V_{FB} = GND	11	12	13	V
V_{STOP}			V_{FB} = GND	7	8	9	
I_{FB}	Feedback Source Current		V_{FB} = GND	0.7	0.9	1.1	mA
$t_{S/S}$	Internal Soft-Start Time[10]		V_{FB} = 4V		10		ms

Electrical Characteristics (Continued)

T_A = 25°C unless otherwise specified.

Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit
Burst-Mode Section							
V_{BURH}	Burst-Mode Voltage		T_J = 25°C	0.5	0.6	0.7	V
V_{BURL}				0.3	0.4	0.5	V
$V_{BUR(HYS)}$				100	200	300	mV
Protection Section							
I_{LIM}	Peak Current Limit	FSQ0170RNA	di/dt = 170mA/µs	0.70	0.80	0.90	A
		FSQ0270RNA	di/dt = 200mA/µs	0.79	0.90	1.01	
t_{CLD}	Current Limit Delay Time(10)				500		ns
T_{SD}	Thermal Shutdown Temperature(10)			125	140		°C
V_{SD}	Shutdown Feedback Voltage			5.5	6.0	6.5	V
V_{OVP}	Over-Voltage Protection			18	19		V
I_{DELAY}	Shutdown Delay Current		V_{FB} = 4V	3.5	5.0	6.5	µA
t_{LEB}	Leading Edge Blanking Time(10)			200			ns
Total Device Section							
I_{OP}	Operating Supply Current (Control Part Only)		V_{CC} = 14V	1	3	5	mA
I_{CH}	Startup Charging Current		V_{CC} = 0V, R_{STR}<100kΩ (12)	0.70	0.85	1.00	mA
V_{STR}	V_{str} Supply Voltage		V_{CC} = 0V		24		V

Notes:

10. These parameters, although guaranteed, are not 100% tested in production.
11. Pulse test: Pulse width ≤ 300µs, duty ≤ 2%.
12. R_{STR} is connected between the rectified AC line voltage source and VSTR pin.

Typical Performance Characteristics (Control Part)

These characteristic graphs are normalized at T_A= 25°C.

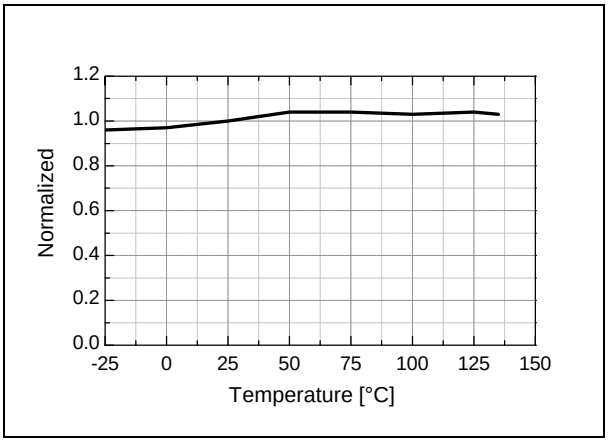


Figure 4. Operating Frequency (f_{OSC}) vs. T_A

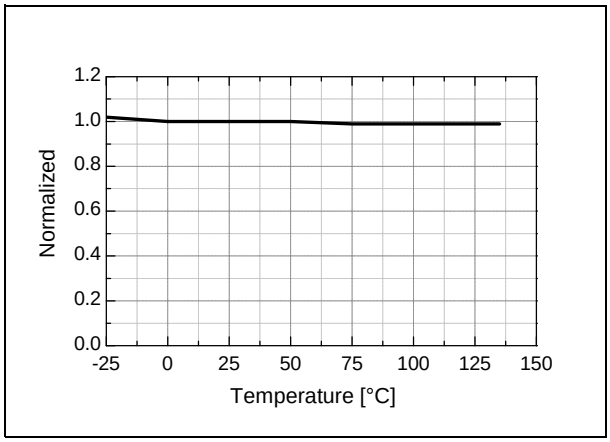


Figure 5. Over-Voltage Protection (V_{OVP}) vs. T_A

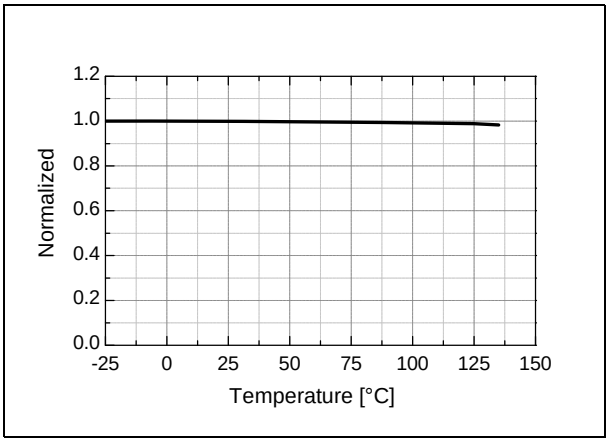


Figure 6. Maximum Duty Cycle (D_{MAX}) vs. T_A

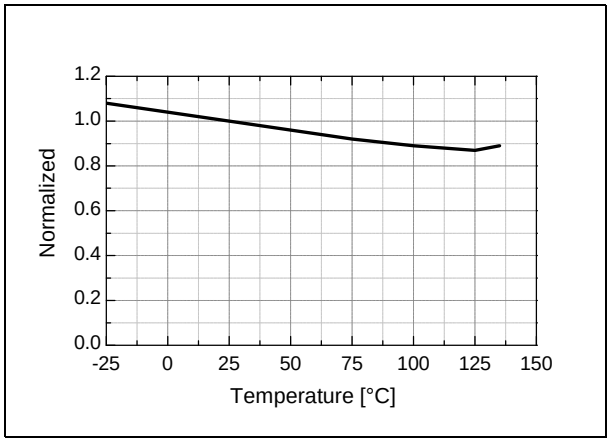


Figure 7. Operating Supply Current (I_{OP}) vs. T_A

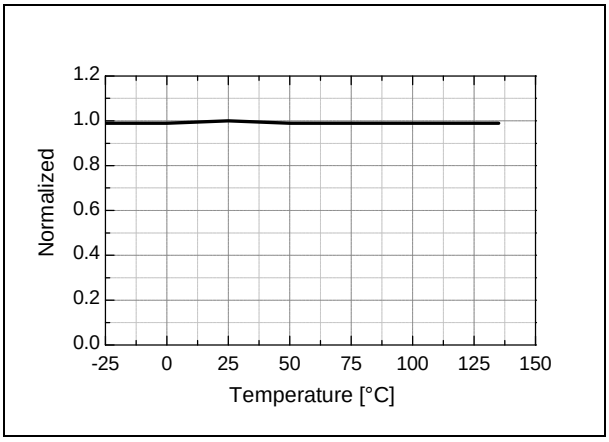


Figure 8. Start Threshold Voltage (V_{START}) vs. T_A

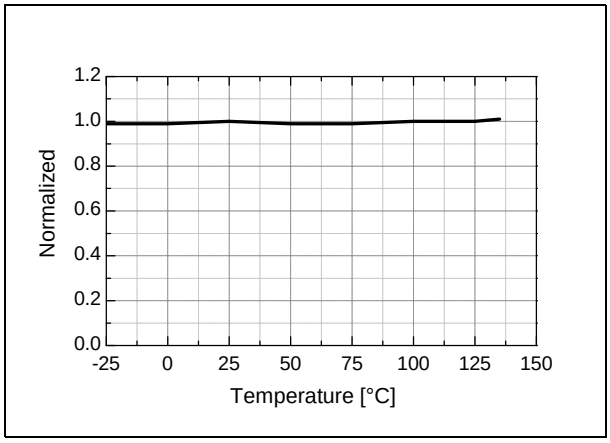


Figure 9. Stop Threshold Voltage (V_{STOP}) vs. T_A

Typical Performance Characteristics (Continued)

These characteristic graphs are normalized at T_A= 25°C.

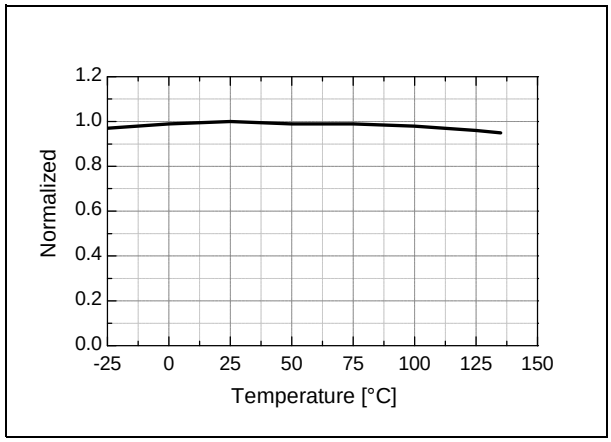


Figure 10. Feedback Source Current (I_{FB}) vs. T_A

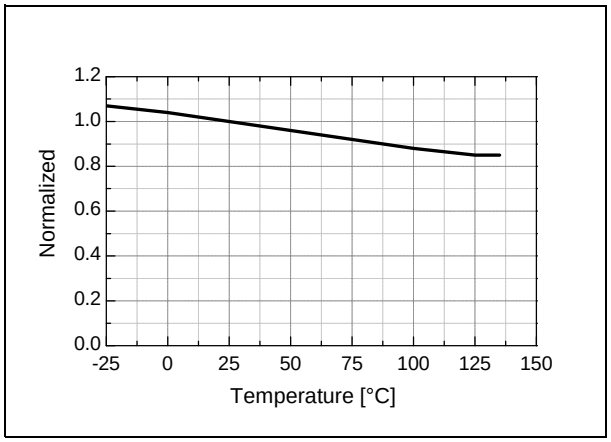


Figure 11. Startup Charging Current (I_{CH}) vs. T_A

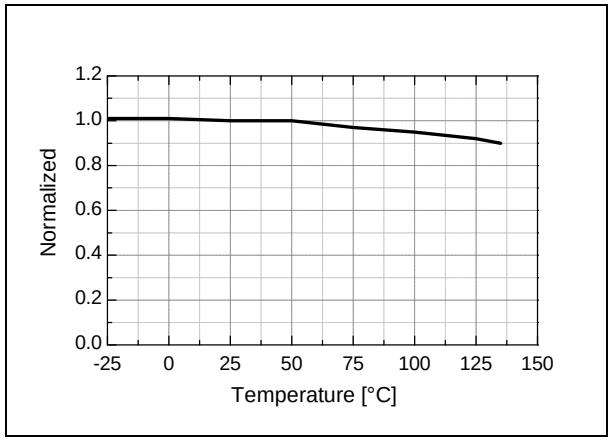


Figure 12. Peak Current Limit (I_{LIM}) vs. T_A

Functional Description

1. Startup: In previous generations of Fairchild Power Switches (FPS™), the V_{str} pin required an external resistor to the DC input voltage line. In this generation, the startup resistor is replaced by an internal high-voltage current source and a switch that shuts off 10ms after the supply voltage, V_{CC}, goes above 12V. The source turns back on if V_{CC} drops below 8V.

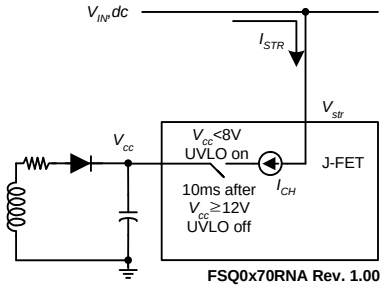


Figure 13. High-Voltage Current Source

2. Feedback Control: The 700V FPS series employs current-mode control, as shown in Figure 14. An opto-coupler (such as the H11A817A) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the R_{sense} resistor of SenseFET, plus an offset voltage, makes it possible to control the switching duty cycle. When the shunt regulator reference pin voltage exceeds the internal reference voltage of 2.5V, the opto-coupler LED current increases, the feedback voltage V_{FB} is pulled down and thereby reduces the duty cycle. This typically happens when the input voltage increases or the output load decreases.

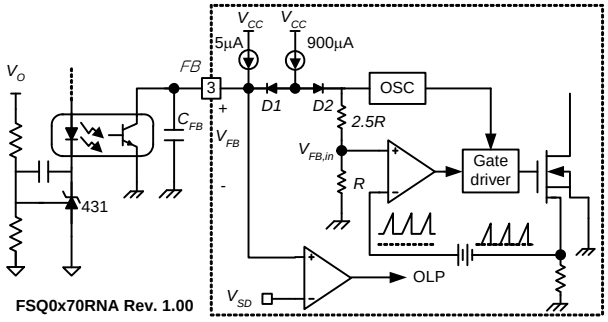


Figure 14. Pulse Width Modulation Circuit

3. Leading Edge Blanking (LEB): When the internal SenseFET is turned on, the primary-side capacitance and secondary-side rectifier diode reverse recovery typically cause a high-current spike through the SenseFET. Excessive voltage across the R_{sense} resistor leads to incorrect feedback operation in the current-mode PWM control. To counter this effect, the FPS employs a Leading Edge Blanking (LEB) circuit. This circuit inhibits the PWM comparator for a short time (t_{LEB}) after the Sense FET is turned on.

4. Protection Circuits: The FPS has several protective functions, such as Overload Protection (OLP), Over-Voltage Protection (OVP), Under-Voltage Lockout (UVLO), and Thermal Shutdown (TSD). Because these protection circuits are fully integrated in the IC without external components, reliability is improved without increasing cost. Once a fault condition occurs, switching is terminated and the SenseFET remains off. This causes V_{CC} to fall. When V_{CC} reaches the UVLO stop voltage, V_{STOP} (typically 8V), the protection is reset and the internal high-voltage current source charges the V_{CC} capacitor via the V_{str} pin. When V_{CC} reaches the UVLO start voltage, V_{START} (typically 12V), the FPS resumes its normal operation. In this manner, the auto-restart can alternately enable and disable the switching of the power SenseFET until the fault condition is eliminated.

4.1 Overload Protection (OLP): Overload is defined as the load current exceeding a pre-set level due to an unexpected event. In this situation, the protection circuit should be activated to protect the SMPS. However, even when the SMPS is operating normally, the OLP circuit can be activated during the load transition. To avoid this undesired operation, the OLP circuit is designed to be activated after a specified time to determine whether it is a transient situation or a true overload situation. In conjunction with the I_{PK} current limit pin (if used), the current mode feedback path limits the current in the SenseFET when the maximum PWM duty cycle is attained. If the output consumes more than this maximum power, the output voltage (V_O) decreases below nominal voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, thus increasing the feedback voltage (V_{FB}). If V_{FB} exceeds 3V, the feedback input diode is blocked and the 5μA current source (I_{DELAY}) starts to slowly charge C_{FB} up to V_{CC}. In this condition, V_{FB} increases until it reaches 6V, when the switching operation is terminated, as shown in Figure 15. The shutdown delay time is the time required to charge C_{FB} from 3V to 6V with 5μA current source.

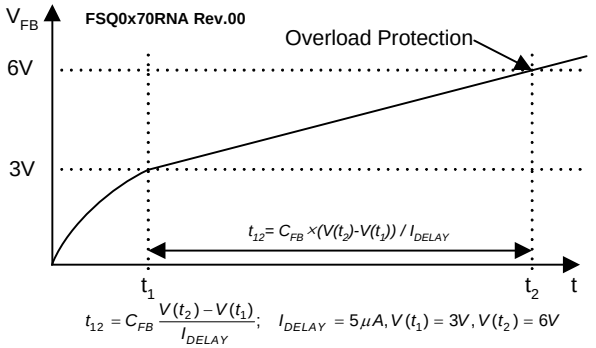


Figure 15. Overload Protection (OLP)

4.2 Thermal Shutdown (TSD): The SenseFET and the control IC are integrated, making it easier for the control

IC to detect the temperature of the SenseFET. When the temperature exceeds approximately 140°C, thermal shutdown is activated.

4.3 Over-Voltage Protection (OVP): In the event of a malfunction in the secondary-side feedback circuit, or an open feedback loop caused by a soldering defect, the current through the opto-coupler transistor becomes almost zero (see Figure 14). V_{FB} climbs up in a similar manner to the overload situation, forcing the preset maximum current to be supplied to the SMPS until the overload protection is activated. Because excess energy is provided to the output, the output voltage may exceed the rated voltage before the overload protection is activated, resulting in the breakdown of the devices in the secondary side. To prevent this situation, an Over-Voltage Protection (OVP) circuit is employed. In general, V_{CC} is proportional to the output voltage and the FPS uses V_{CC} instead of directly monitoring the output voltage. If V_{CC} exceeds 19V, the OVP circuit is activated, resulting in termination of the switching operation. To avoid undesired activation of OVP during normal operation, V_{CC} should be designed to be below 19V.

5. Soft-Start: The FPS has an internal soft-start circuit that slowly increases the SenseFET current after start-up, as shown in Figure 16. The typical soft-start time is 10ms, where progressive increments of the SenseFET current are allowed during the start-up phase. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased to smoothly establish the required output voltage. This also helps prevent transformer saturation and reduces the stress on the secondary diode during startup.

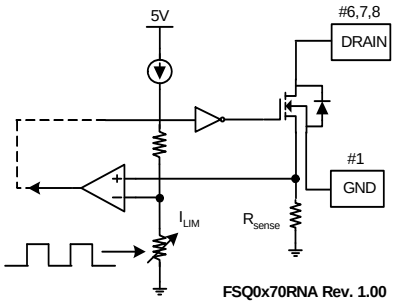


Figure 16. Soft-Start Function

6. Burst Operation: To minimize power dissipation in standby mode, the FPS enters burst-mode operation. Feedback voltage decreases as the load decreases, as shown in Figure 17, and the device automatically enters burst-mode when the feedback voltage drops below V_{BURH} (typically 600mV). Switching continues until the feedback voltage drops below V_{BURL} (typically 400mV). At this point, switching stops and the output voltage starts to drop at a rate dependent on the standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH}, switching resumes. The feedback voltage then falls and the process is repeated. Burst-mode operation alternately enables and disables switching of the SenseFET and reduces switching loss in standby mode.

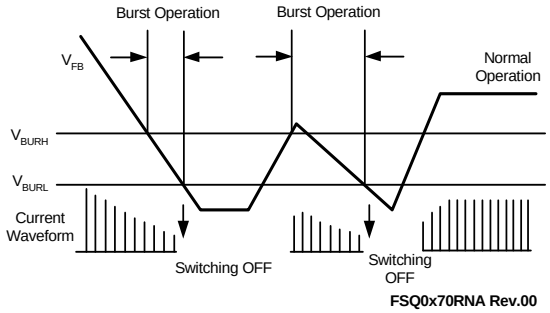


Figure 17. Burst Operation Function

7. Adjusting Peak Current Limit: As shown in Figure 18, a combined 2.8kΩ internal resistance is connected to the non-inverting lead on the PWM comparator. An external resistance of Rx on the current limit pin forms a parallel resistance with the 2.8kΩ when the internal diodes are biased by the main current source of 900μA.

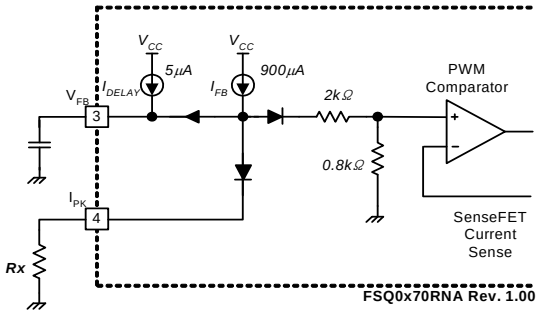


Figure 18. Peak Current Limit Adjustment

For example, FSQ0270RNA has a typical SenseFET peak current limit (I_{LIM}) of 0.9A. I_{LIM} can be adjusted to 0.6A by inserting Rx between the I_{PK} pin and the ground. The value of the Rx can be estimated by the following equations:

0.9A: 0.6A = 2.8kΩ : XkΩ,

X = Rx || 2.8kΩ

where X represents the resistance of the parallel network.

Application Information

Methods of Reducing Audible Noise

Switching-mode power converters have electronic and magnetic components, which generate audible noise when the operating frequency is in the range of 20~20,000Hz. Even though they operate above 20KHz, they can make noise, depending on the load condition. The following sections discuss methods to reduce noise.

Glue or Varnish

The most common method of reducing noise involves using glue or varnish to tighten magnetic components. The motion of core, bobbin, and coil and the chattering or magnetostriction of core can cause the transformer to produce audible noise. The use of rigid glue and varnish helps reduce the transformer noise. Glue or varnish can also can crack the core because sudden changes in the ambient temperature cause the core and the glue to expand or shrink in a different ratio.

Ceramic Capacitor

Using a film capacitor instead of a ceramic capacitor as a snubber capacitor is another noise reduction solution. Some dielectric materials show a piezoelectric effect, depending on the electric field intensity. Hence, a snubber capacitor becomes one of the most significant sources of audible noise. Another possibility is to use a Zener clamp circuit instead of an RCD snubber for higher efficiency as well as lower audible noise.

Adjusting Sound Frequency

Moving the fundamental frequency of noise out of the 2~4kHz range is the third method. Generally, humans are more sensitive to noise in the range of 2~4kHz. When the fundamental frequency of noise is located in this range, the noise sounds louder although the noise intensity level is identical (see Figure 19).

When the FPS acts in burst mode and the burst operation is suspected to be a source of noise, this method may be helpful. If the frequency of burst mode operation lies in the range of 2~4kHz, adjusting the feedback loop can shift the burst operation frequency. To reduce the burst operation frequency, increase a feedback gain capacitor (C_F), opto-coupler supply resistor (R_D); and feedback capacitor (C_B), and decrease a feedback gain resistor (R_F), as shown in Figure 20.

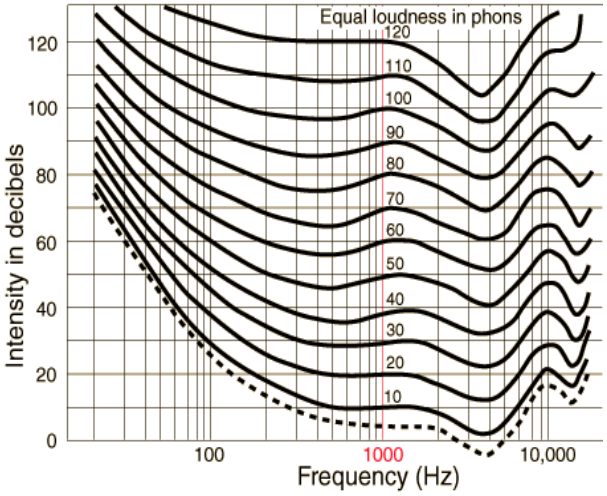


Figure 19. Equal Loudness Curves

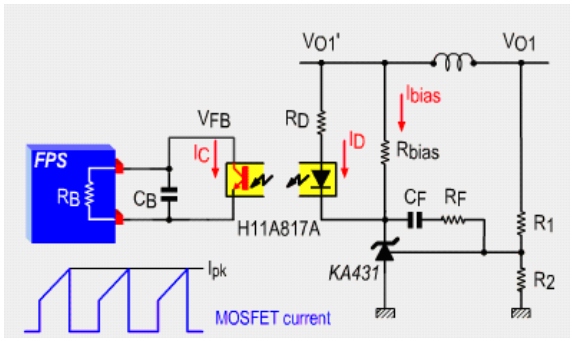


Figure 20. Typical Feedback Network of FPS

Other Reference Materials

AN-4134: Design Guidelines for Off-line Forward Converters Using Fairchild Power Switch (FPS™)

AN-4137: Design Guidelines for Off-line Flyback Converters Using Fairchild Power Switch (FPS™)

AN-4140: Transformer Design Consideration for Off-line Flyback Converters using Fairchild Power Switch (FPS™)

AN-4141: Troubleshooting and Design Tips for Fairchild Power Switch (FPS™) Flyback Applications

AN-4147: Design Guidelines for RCD Snubber of Flyback

AN-4148: Audible Noise Reduction Techniques for FPS™ Applications

Typical Application Circuit

Application	Output power	Input Voltage	Output Voltage (Max. Current)
PC Auxiliary Power Supply (Using FSQ0270RNA)	15W	Universal input (85-265 V_{AC})	5V (3A)

Features

- High efficiency (> 78% at 115 V_{AC} and 230 V_{AC} input)
- Low standby mode power consumption (< 0.8W at 230 V_{AC} input and 0.5W load)
- Enhanced system reliability through various protection functions
- Internal soft-start (10ms)
- Line UVLO function can be achieved using external component

Key Design Notes

- The delay time for overload protection is designed to be about 30ms with C8 of 47nF. If faster/slower triggering of OLP is required, C8 can be changed to a smaller/larger value (e.g. 100nF for about 60ms).
- ZP1, DL1, RL1, RL2, RL3, RL4, RL5, RL7, QL1, QL2, and CL9 build a Line Under-Voltage Lockout block (UVLO). The Zener voltage of ZP1 determines the input voltage that makes FPS turn on. RL5 and DL1 provide a reference voltage from V_{CC}. If the input voltage divided by RL1, RL2, and RL4 is lower than the Zener voltage of DL1, QL1 and QL2 turn on and pull down V_{FB} to ground.
- An evaluation board and corresponding test report can be provided.

1. Schematic

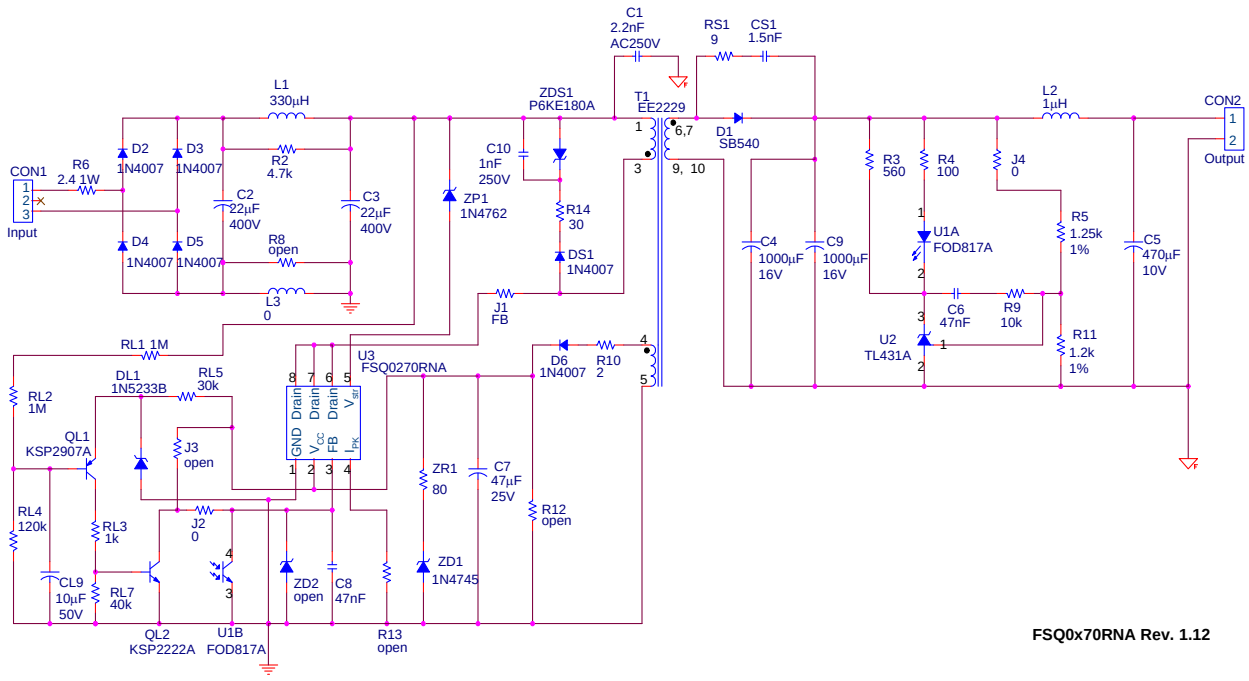


Figure 21. Demo Circuit

2. Transformer

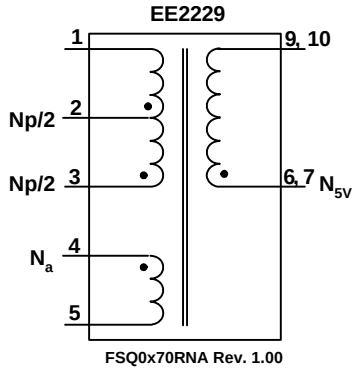


Figure 22. Transformer Schematic Diagram

3. Winding Specification

	Pin (S → F)	Wire	Turns	Winding Method
$N_p/2$	3 → 2	0.3φ × 1	72	Solenoid winding
Insulation: Polyester Tape t = 0.025mm, 1 Layers				
N_a	4 → 5	0.25φ × 2	22	Solenoid winding
Insulation: Polyester Tape t = 0.025mm, 2 Layers				
N_{5V}	6, 7 → 9, 10	0.65φ × 2	8	Solenoid winding
Insulation: Polyester Tape t = 0.025mm, 2 Layers				
$N_p/2$	2 → 1	0.3φ × 1	72	Solenoid winding
Insulation: Polyester Tape t = 0.025mm, 2 Layers				

4. Electrical Characteristics

	Pin	Specification	Remark
Inductance	1–3	1.20mH ± 5%	100kHz, 1V
Leakage	1–3	< 30μH Max	Short all other pins

5. Core & Bobbin

- Core: EE2229 (Material: PL-7, Ae = 35.7 mm^2)
- Bobbin: BE2229

6. Demo Circuit Part List

Part Number	Value	Quantity	Description (Manufacturer)
C6, C8	47nF	2	Ceramic Capacitor
C1	2.2nF (1KV)	1	AC Ceramic Capacitor(X1 & Y1)
C10	1nF (200V)	1	Mylar Capacitor
CS1	1.5nF (50V)	1	Ceramic Capacitor
C2, C3	22µF (400V)	2	Low Impedance Electrolytic Capacitor KMX series
C4, C9	1000µF (16V)	2	Low ESR Electrolytic Capacitor NXC series
C5	470µF (10V)	1	Low ESR Electrolytic Capacitor NXC series
C7	47µF (25V)	1	General Electrolytic Capacitor
CL9	10µF (50V)	1	General Electrolytic Capacitor
L1	330µH	1	Inductor
L2	1µH	1	Inductor
R6	2.4 (1W)	1	Fusible Resistor
J1, J2, J4, L3	0	4	Jumper
R2	4.7kΩ	1	Resistor
R3	560Ω	1	Resistor
R4	100Ω	1	Resistor
R5	1.25kΩ	1	Resistor
R11	1.2kΩ	1	Resistor
R9	10kΩ	1	Resistor
R10	2Ω	1	Resistor
R14	30Ω	1	Resistor
RL3	1kΩ	1	Resistor
RL1, RL2	1MΩ	2	Resistor
RL4	120kΩ	1	Resistor
RL5	30kΩ	1	Resistor
RL7	40kΩ	1	Resistor
RS1	9Ω	1	Resistor
ZR1	80Ω	1	Resistor
U1	FOD817A	1	IC (Fairchild Semiconductor)
U2	TL431	1	IC (Fairchild Semiconductor)
U3	FSQ0270RNA	1	IC (Fairchild Semiconductor)
QL1	2N2907	1	IC (Fairchild Semiconductor)
QL2	2N2222	1	IC (Fairchild Semiconductor)
D2, D3, D4, D5, D6, DS1	1N4007	6	Diode (Fairchild Semiconductor)
D1	SB540	1	Schottky Diode (Fairchild Semiconductor)
ZD1	1N4745	1	Zener Diode (Fairchild Semiconductor)
DL1	1N5233	1	Zener Diode (Fairchild Semiconductor)
ZP1	82V (1W)	1	Zener Diode (Fairchild Semiconductor)
ZDS1	P6KE180A	1	TVS (Fairchild Semiconductor)

7. Layout

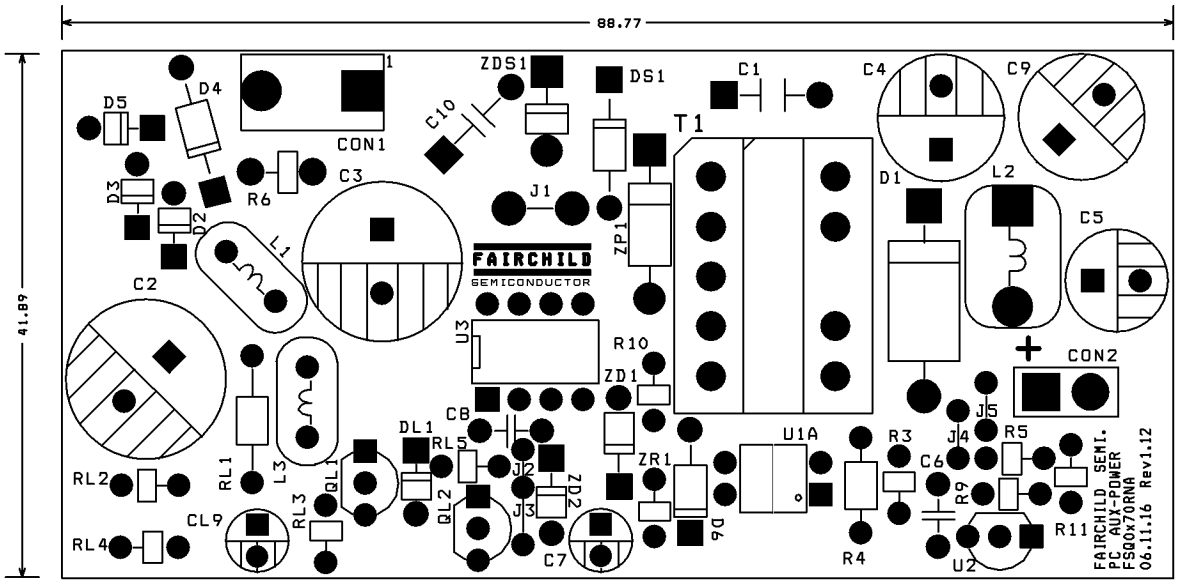


Figure 23. Top Image of PCB

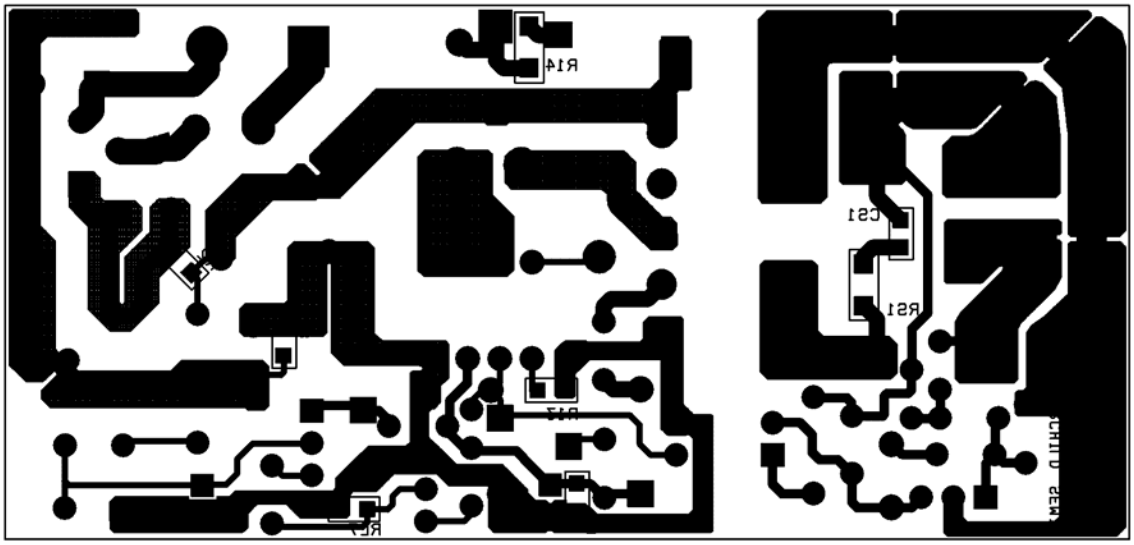
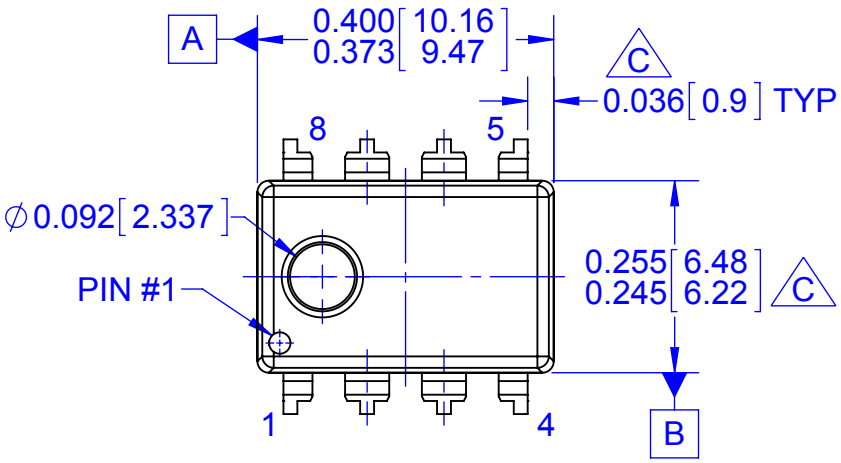
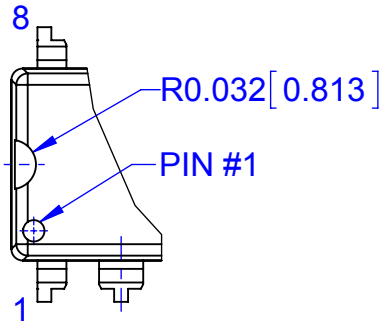


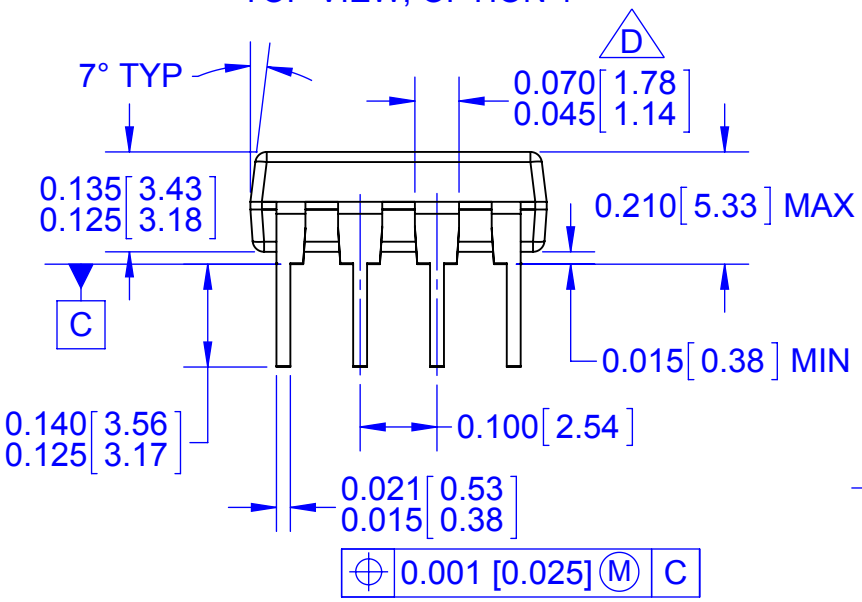
Figure 24. Bottom Image of PCB



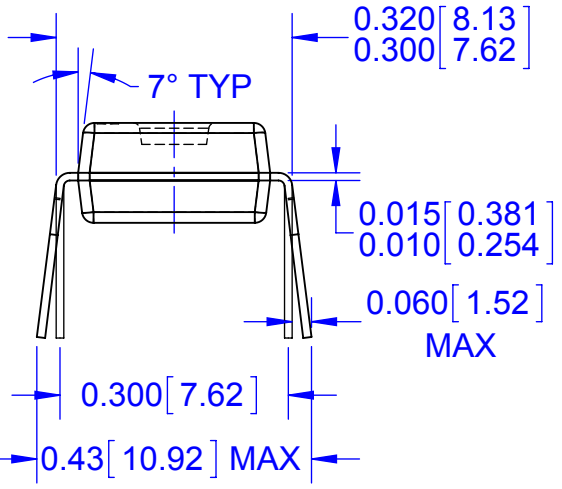
TOP VIEW, OPTION 1



TOP VIEW, OPTION 2



FRONT VIEW



SIDE VIEW

NOTES:

A. CONFORMS TO JEDEC MS-001, VARIATION BA

B. CONTROLLING DIMENSIONS ARE IN INCHES.
REFERENCE DIMENSIONS ARE IN MILLIMETERS.

C DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED
0.010 INCHES OR 0.25MM.

D DOES NOT INCLUDE DAMBAR PROTRUSIONS.
DAMBAR PROTRUSIONS SHALL NOT EXCEED 0.010
INCHES OR 0.25MM.

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