

KA5Q0740RT

Fairchild Power Switch(FPS)

Features

- Quasi Resonant Converter Controller
- Internal Burst Mode Controller for Stand-by Mode
- Pulse by Pulse Current Limiting
- Over Current Latch Protection
- Over Voltage Protection (Vsync: Min. 11V)
- Internal Thermal Shutdown Function
- Under Voltage Lockout
- Internal High Voltage Sense FET
- Auto-Restart Mode

Description

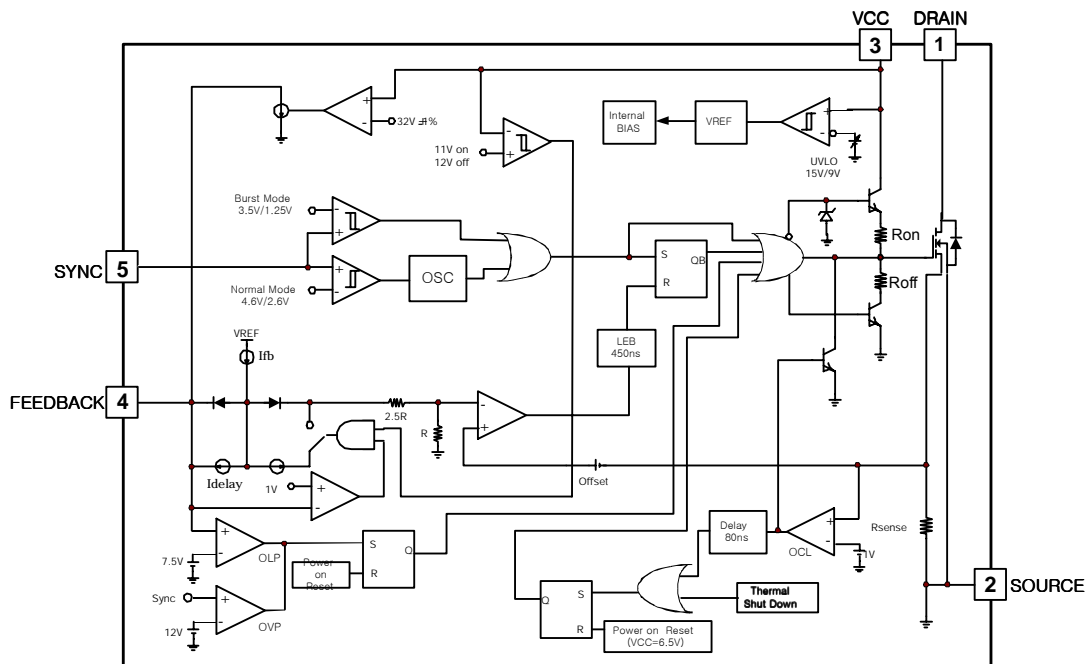
The Fairchild Power Switch(FPS) product family is specially designed for an off-line SMPS with minimal external components. The Fairchild Power Switch(FPS) consists of a high voltage power SenseFET and a current mode PWM IC. The integrated PWM controller includes the fixed oscillator, the under voltage lock out, the leading edge blanking, the optimized gate turn-on/turn-off driver, the thermal shut down protection, the over voltage protection, and the temperature compensated precision current sources for loop compensation and fault protection circuitry. Compared to a discrete MOSFET and a controller or a RCC switching converter solutions, a Fairchild Power Switch(FPS) can reduce the total number of components, design size, and weight, so it will improve efficiency, productivity, and system reliability. It has a basic platform well suited for cost-effective design in a quasi-resonant converter as a C-TV power supply.

TO-220F-5L



1. Drain
2. GND
3. VCC
4. Feedback
5. Sync

Internal Block Diagram



Rev.1.0.5

Absolute Maximum Ratings

(Ta=25°C, unless otherwise specified)

| Parameter | Symbol | Value | Unit |
|--|-----------------------|-------------------------|-------|
| Drain-source Voltage | V _{DSS} | 400 | V |
| Drain-Gate Voltage (R _{GS} =1MΩ) | V _{DGR} | 400 | V |
| Gate-Source (GND) Voltage | V _{GS} | ±30 | V |
| Drain Current Pulsed ⁽²⁾ | I _{DM} | 18.4 | ADC |
| Single Pulsed Avalanch Current ⁽³⁾ (Energy ⁽²⁾) | I _{AS} (EAS) | 20(360) | A(mJ) |
| Continuous Drain Current (T _c = 25°C) | I _D | 4.6 | ADC |
| Continuous Drain Current (T _C =100°C) | I _D | 2.9 | ADC |
| Supply Voltage | V _{CC} | 40 | V |
| Analog Input Voltage Range | V _{sync} | -0.3 to 13V | V |
| | V _{FB} | -0.3 to V _{CC} | V |
| Total Power Dissipation | P _D | 42 | W |
| | Derating | 0.33 | W/°C |
| Operating Junction Temperature | T _J | +160 | °C |
| Operating Ambient Temperature | T _A | -25 to +85 | °C |
| Storage Temperature Range | T _{STG} | -55 to +150 | °C |
| Thermal Resistance | R _{thjc} | 2.98 | °C/W |
| ESD Capability, HBM Model (All pins) | - | 2.0 | kV |
| ESD Capability, Machine Model (All pins) | - | 300 | V |

Notes:

1. T_j = 25°C to 150°C
2. Repetitive rating: Pulse width limited by maximum junction temperature
3. L = 30mH, V_{DD} = 50V, R_G = 25Ω, starting T_j = 25°C
4. L = 13uH, starting T_j = 25°C

Electrical Characteristics (SFET Part)

(Ta=25°C unless otherwise specified)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---------------------|--|------|------|------|------|
| Drain-Source Breakdown Voltage | BV _{DSS} | V _{GS} = 0V, I _D = 50μA | 400 | - | - | V |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{DS} = Max, Rating, V _{GS} = 0V | - | - | 200 | μA |
| | | V _{DS} = 0.8*Max., Rating V _{GS} = 0V, T _C = 85°C | - | - | 300 | μA |
| Static Drain-source on Resistance ^(Note) | R _{DS(ON)} | V _{GS} = 10V, I _D = 2.3A | - | 0.9 | 1.1 | Ω |
| Input Capacitance | C _{iss} | V _{GS} = 0V, V _{DS} = 25V, f = 1MHz | - | 710 | - | pF |
| Output Capacitance | C _{oss} | | - | 90 | - | |
| Reverse Transfer Capacitance | C _{rss} | | - | 10 | - | |
| Turn on Delay Time | t _{d(on)} | V _{DD} = 0.5BV _{DSS} , I _D = 7.0A (MOSFET switching time are essentially independent of operating temperature) | - | 15 | - | nS |
| Rise Time | t _r | | - | 55 | - | |
| Turn Off Delay Time | t _{d(off)} | | - | 55 | - | |
| Fall Time | t _f | | - | 50 | - | |
| Total Gate Charge (Gate-Source+Gate-Drain) | Q _g | V _{GS} = 10V, I _D = 7.0A, V _{DS} = 0.5B V _{DSS} (MOSFET Switching time are Essentially independent of operating temperature) | - | 20 | 26 | nC |
| Gate-Source Charge | Q _{gs} | | - | 4.0 | - | |
| Gate-Drain (Miller) Charge | Q _{gd} | | - | 7.3 | - | |

Note:

1. Pulse test : Pulse width ≤ 300μS, duty ≤ 2%

Electrical Characteristics (Continued)

(Ta=25°C unless otherwise specified)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|------------------------------------|--------------------|-----------------------------|------|------|------|------|
| UVLO SECTION | | | | | | |
| Start Threshold Voltage | VSTART | V _{FB} = GND | 14 | 15 | 16 | V |
| Stop Threshold Voltage | VSTOP | V _{FB} = GND | 8 | 9 | 10 | V |
| OSCILLATOR SECTION | | | | | | |
| Initial Frequency | FOSC | - | 18 | 20 | 22 | kHz |
| Voltage Stability | FSTABLE | 12V ≤ V _{CC} ≤ 23V | 0 | 1 | 3 | % |
| Temperature Stability (Note2) | ΔFOSC | -25°C ≤ Ta ≤ 85°C | 0 | ±5 | ±10 | % |
| Maximum Duty Cycle | DMAX | - | 92 | 95 | 98 | % |
| Minimum Duty Cycle | DMIN | - | - | - | 0 | % |
| FEEDBACK SECTION | | | | | | |
| Feedback Source Current | I _{FB} | V _{FB} = GND | 0.7 | 0.9 | 1.1 | mA |
| Shutdown Feedback Voltage | V _{SD} | V _{fb} ≥ 6.9V | 6.9 | 7.5 | 8.1 | V |
| Shutdown Delay Current | I _{DELAY} | V _{FB} = 5V | 4 | 5 | 6 | μA |
| PROTECTION SECTION | | | | | | |
| Over Voltage Protection | VOVP | V _{sync} ≥ 11V | 11 | 12 | 13 | V |
| Over Current Latch Voltage (Note2) | VOCL | - | 0.9 | 1.0 | 1.1 | V |
| Thermal Shutdown Temp. | TSD | - | 140 | 160 | - | °C |

Note:

1. These parameters is the current flowing in the Control IC.
2. These parameters, although guaranteed, are tested in EDS(wafer test) process.
3. These parameters indicate Inductor Current.

Electrical Characteristics (Continued)

(Ta=25°C unless otherwise specified)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|--|----------------------|-----------------------------------|------|------|------|------|
| SYNC SECTION | | | | | | |
| Normal Sync High Threshold Voltage | VNSH | Vcc = 16V, Vfb = 5V | 4.0 | 4.6 | 5.2 | V |
| Normal Sync Low Threshold Voltage | VNSL | Vcc = 16V, Vfb = 5V | 2.3 | 2.6 | 2.9 | V |
| Burst Sync High Threshold Voltage | VBSH | Vcc = 10.5V, Vfb = 0V | 3.2 | 3.6 | 4.0 | V |
| Burst Sync Low Threshold Voltage | VBSL | Vcc = 10.5V, Vfb = 0V | 1.1 | 1.3 | 1.5 | V |
| BURST MODE SECTION | | | | | | |
| Burst mode Low Threshold Voltage | VBURL | Vfb = 0V | 10.4 | 11.0 | 11.6 | V |
| Burst mode High Threshold Voltage | VBURH | Vfb = 0V | 11.4 | 12.0 | 12.6 | V |
| Burst mode Enable Feedback Voltage | VBEN | Vcc = 10.5V | 0.7 | 1.0 | 1.3 | V |
| Burst mode Peak Current Limit | IBU_PK | Vcc = 10.5V | 0.65 | 0.85 | 1.1 | A |
| PRIMARY SIDE REGULATION SECTION | | | | | | |
| Primary Regulation Threshold Voltage | VPR | I _{fb} = 700uA, Vfb = 4V | 32.0 | 32.5 | 33.0 | V |
| Primary Regulation Transconductance | GPR | - | 2.0 | 2.6 | - | mA/V |
| CURRENT LIMIT(SELF-PROTECTION)SECTION | | | | | | |
| Peak Current Limit(Note3) | IPK | - | 4.4 | 5.0 | 5.6 | A |
| TOTAL DEVICE SECTION | | | | | | |
| Start Up Current | ISTART | Vfb = GND, VCC = 14V | - | 0.1 | 0.2 | mA |
| Operating Supply Current (Note1) | I _{OP} | Vfb = GND, VCC = 16V | - | 10 | 18 | mA |
| | I _{OP(MIN)} | Vfb = GND, VCC = 10V | | | | |
| | I _{OP(MAX)} | Vfb = GND, VCC = 28V | | | | |

Note:

1. These parameters is the current flowing in the Control IC.
2. These parameters, although guaranteed, are tested in EDS(wafer test) process.
3. These parameters indicate Inductor Current.

Typical Performance Characteristics

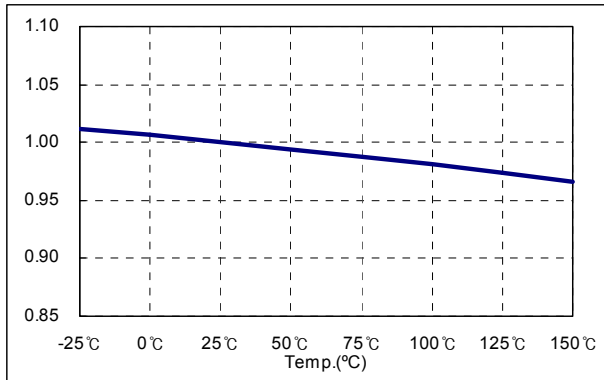


Figure 1. Start Voltage

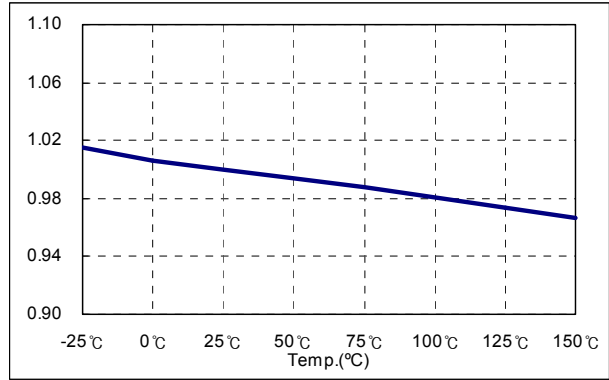


Figure 2. Stop Voltage

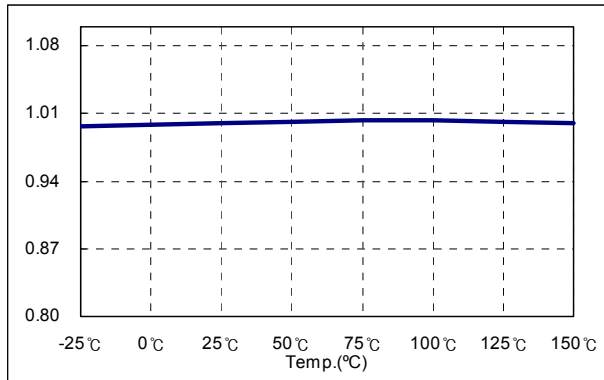


Figure 3. Stand by Current

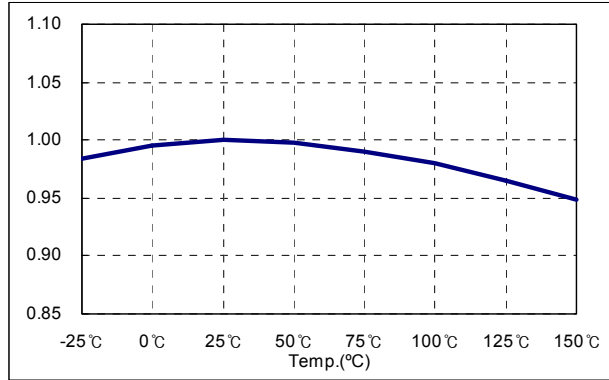


Figure 4. Operating Current

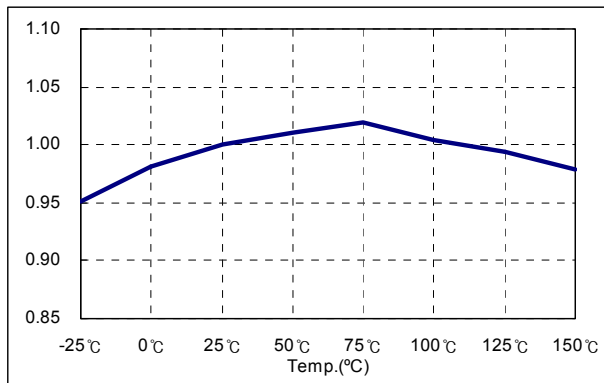


Figure 5. Initial Frequency

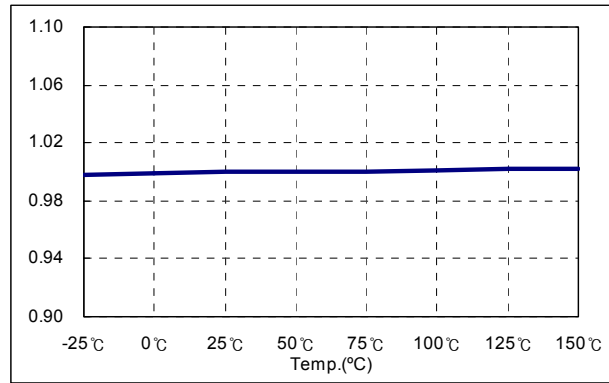


Figure 6. Maximum Duty

Typical Performance Characteristics (Continued)

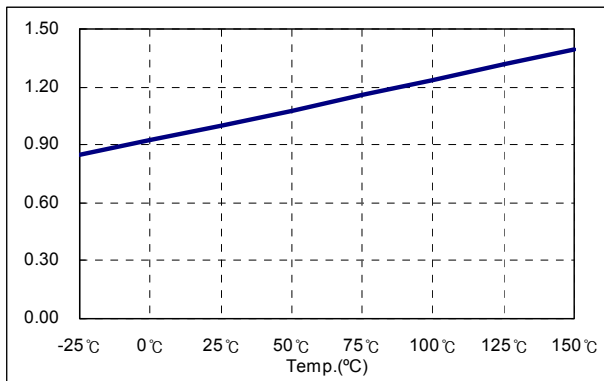


Figure 7. Feedback Offset Voltage

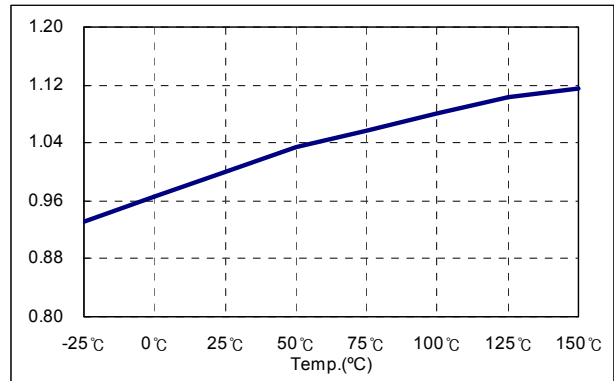


Figure 8. Feedback Source Current

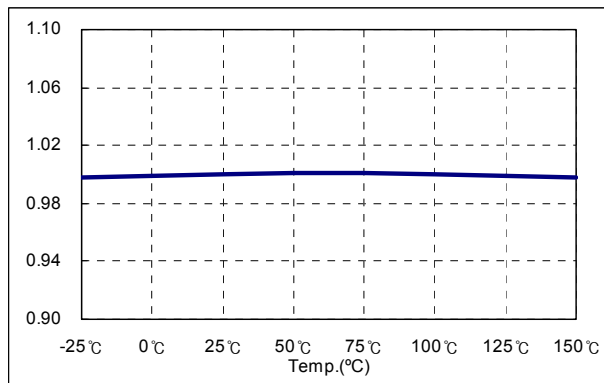


Figure 9. Over Voltage Protection

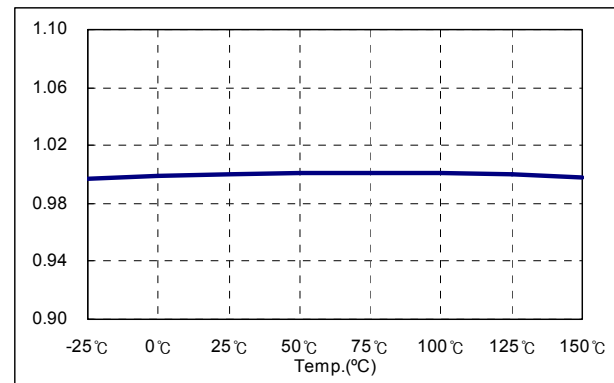


Figure 10. Shutdown Feedback Voltage

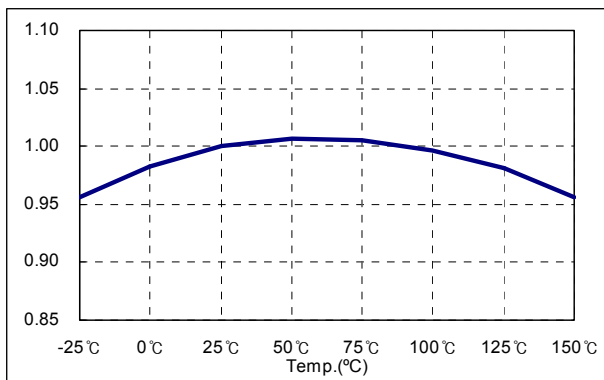


Figure 11. ShutDown Delay Current

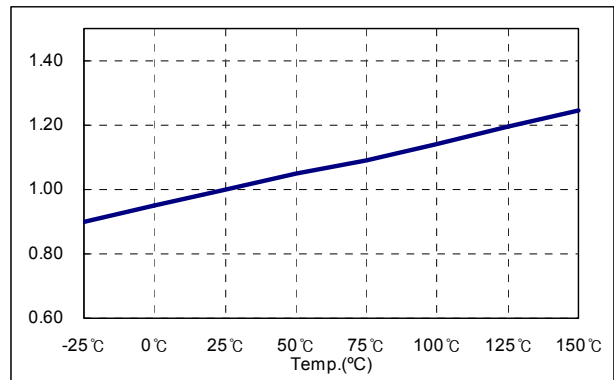


Figure 12. Burst Mode Enable Feedback Voltage

Typical Performance Characteristics (Continued)

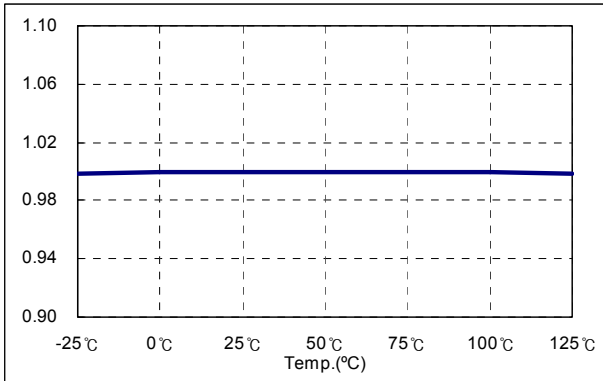


Figure 13. Burst Mode Low Threshold Voltage

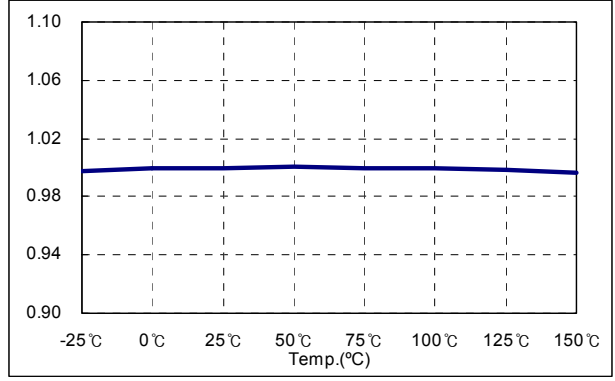


Figure 14. Burst Mode High Threshold Voltage

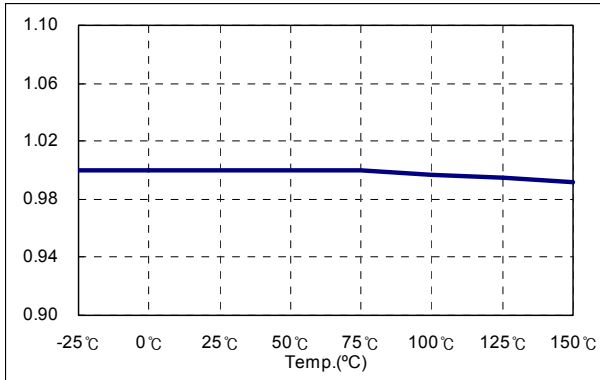


Figure 15. Burst Mode Sync. High Threshold Voltage

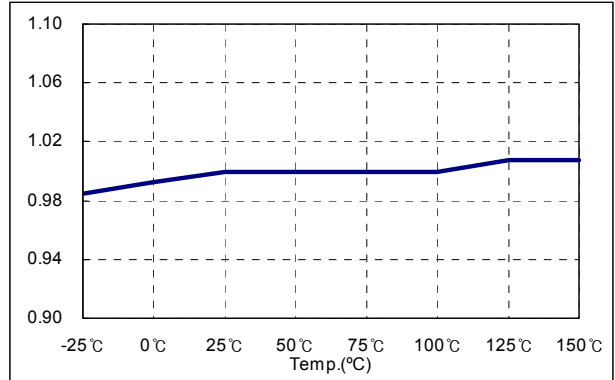


Figure 16. Burst Mode Sync. Low Threshold Voltage

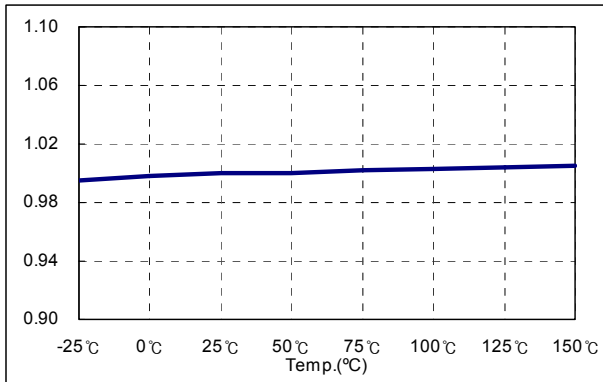


Figure 17. Primary Voltage

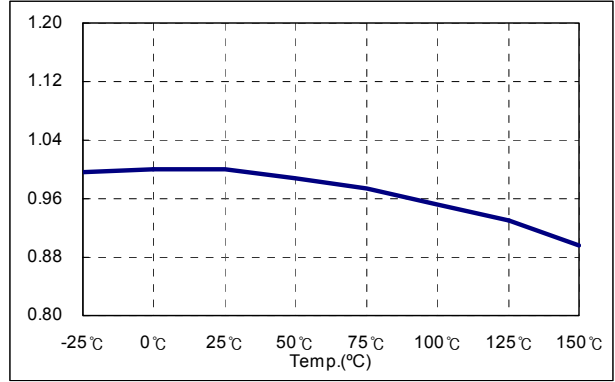


Figure 18. Primary Mode Gain

Typical Performance Characteristics (Continued)

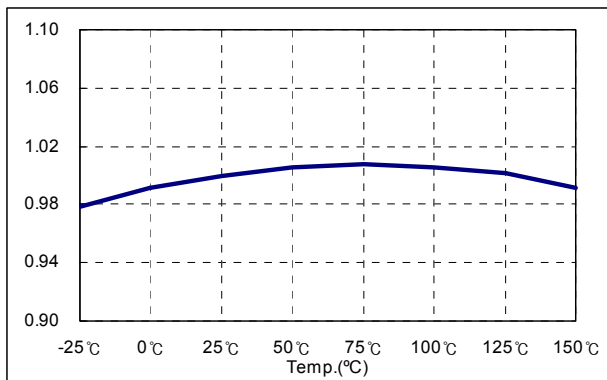


Figure 19. Peak Current Limit

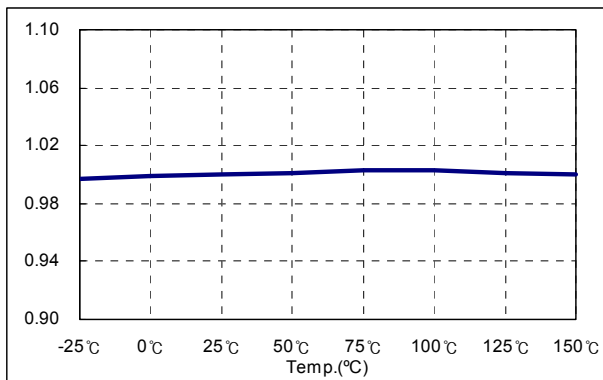


Figure 20. Burst Mode Peak Current Limit

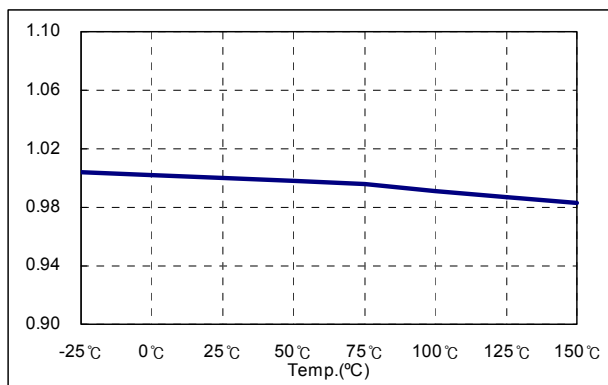


Figure 21. Normal Mode Sync. High Threshold Voltage

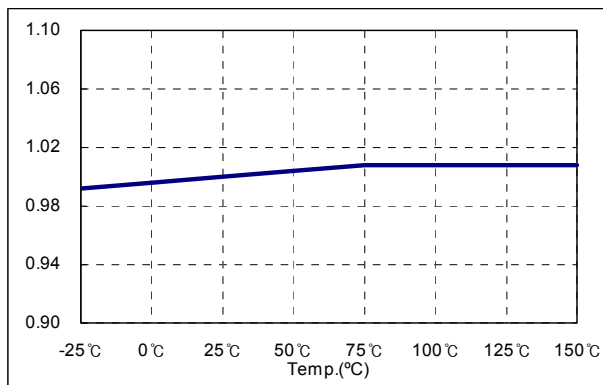


Figure 21. Normal Mode Sync. Low Threshold Voltage

Typical Performance Characteristics(MOSFET Part)

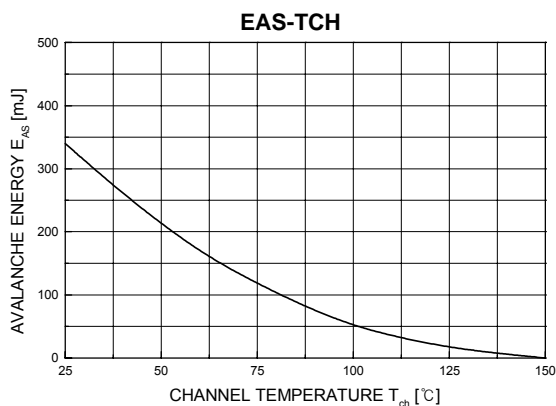


Figure 22. Temperature (T_C) vs. Eas Curve

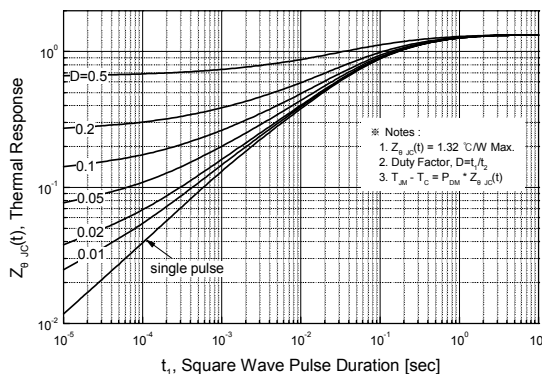
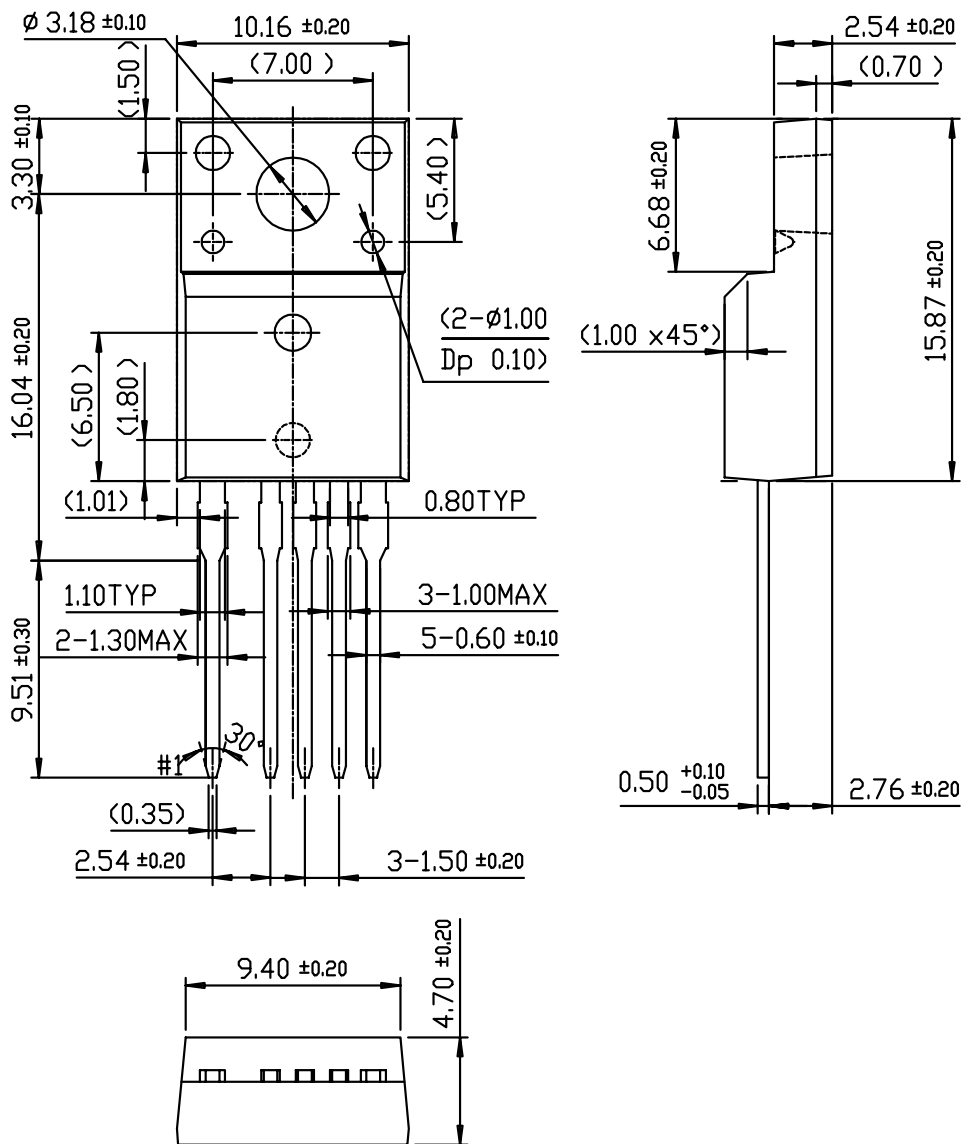


Figure 23. Transient Thermal Response Curve

Package Dimensions

TO-220F-5L



Ordering Information

| Product Number | Package | Operating Temp. |
|----------------|---------------------|-----------------|
| KA5Q0740RTTU | TO-220F-5L | -25°C to +85°C |
| KA5Q0740RTYDTU | TO-220F-5L(Forming) | |

TU : Non Forming Type

YDTU : Forming Type

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