



FSD156MRBN

Green-Mode Fairchild Power Switch (FPS™)

Features

- Advanced Soft Burst-Mode Operation for Low Standby Power and Low Audible Noise
- Random Frequency Fluctuation (RFF) for Low EMI
- Pulse-by-Pulse Current Limit
- Various Protection Functions: Overload Protection (OLP), Over-Voltage Protection (OVP), Abnormal Over-Current Protection (AOCP), Internal Thermal Shutdown (TSD) with Hysteresis, Output-Short Protection (OSP), and Under-Voltage Lockout (UVLO) with Hysteresis
- Low Operating Current (0.4mA) in Burst Mode
- Internal Startup Circuit
- Internal High-Voltage SenseFET: 650V
- Built-in Soft-Start: 15ms
- Auto-Restart Mode

Description

The FSD156MRBN is an integrated Pulse Width Modulation (PWM) controller and SenseFET specifically designed for offline Switch-Mode Power Supplies (SMPS) with minimal external components. The PWM controller includes an integrated fixed-frequency oscillator, Under-Voltage Lockout (UVLO), Leading-Edge Blanking (LEB), optimized gate driver, internal soft-start, temperature-compensated precise current sources for loop compensation, and self-protection circuitry. Compared with a discrete MOSFET and PWM controller solution, the FSD series can reduce total cost, component count, size, and weight; while simultaneously increasing efficiency, productivity, and system reliability. This device provides a basic platform suited for cost-effective design of a flyback converter.

Applications

- Power Supply for LCD Monitor, STB, and DVD Combination

Ordering Information

Part Number	Package	Operating Junction Temperature	Current Limit	R _{DS(ON)} (Max.)	Output Power Table ⁽²⁾				Replaces Device
					230V _{AC} ±15% ⁽³⁾		85-265V _{AC}		
					Adapter ⁽⁴⁾	Open Frame ⁽⁵⁾	Adapter ⁽⁴⁾	Open Frame ⁽⁵⁾	
FSD156MRBN	8-DIP	-40°C ~ +125°C	1.60A	2.3Ω	26W	40W	20W	30W	FSFM300N FSGM300

Notes:

1. Lead-free package per JEDEC J-STD-020B.
2. The junction temperature can limit the maximum output power.
3. 230V_{AC} or 100/115V_{AC} with voltage doubler.
4. Typical continuous power in a non-ventilated enclosed adapter measured at 50°C ambient temperature.
5. Maximum practical continuous power in an open-frame design at 50°C ambient temperature.

Application Circuit

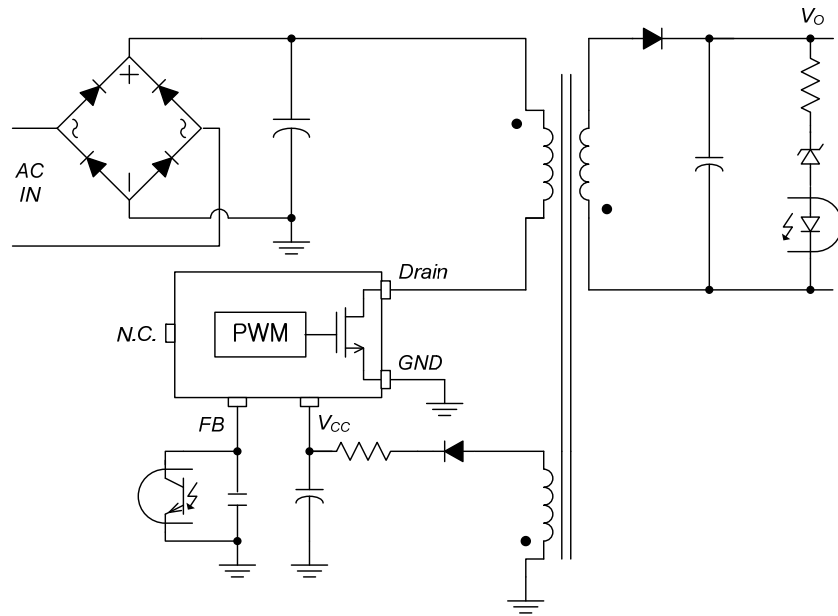


Figure 1. Typical Application Circuit

Internal Block Diagram

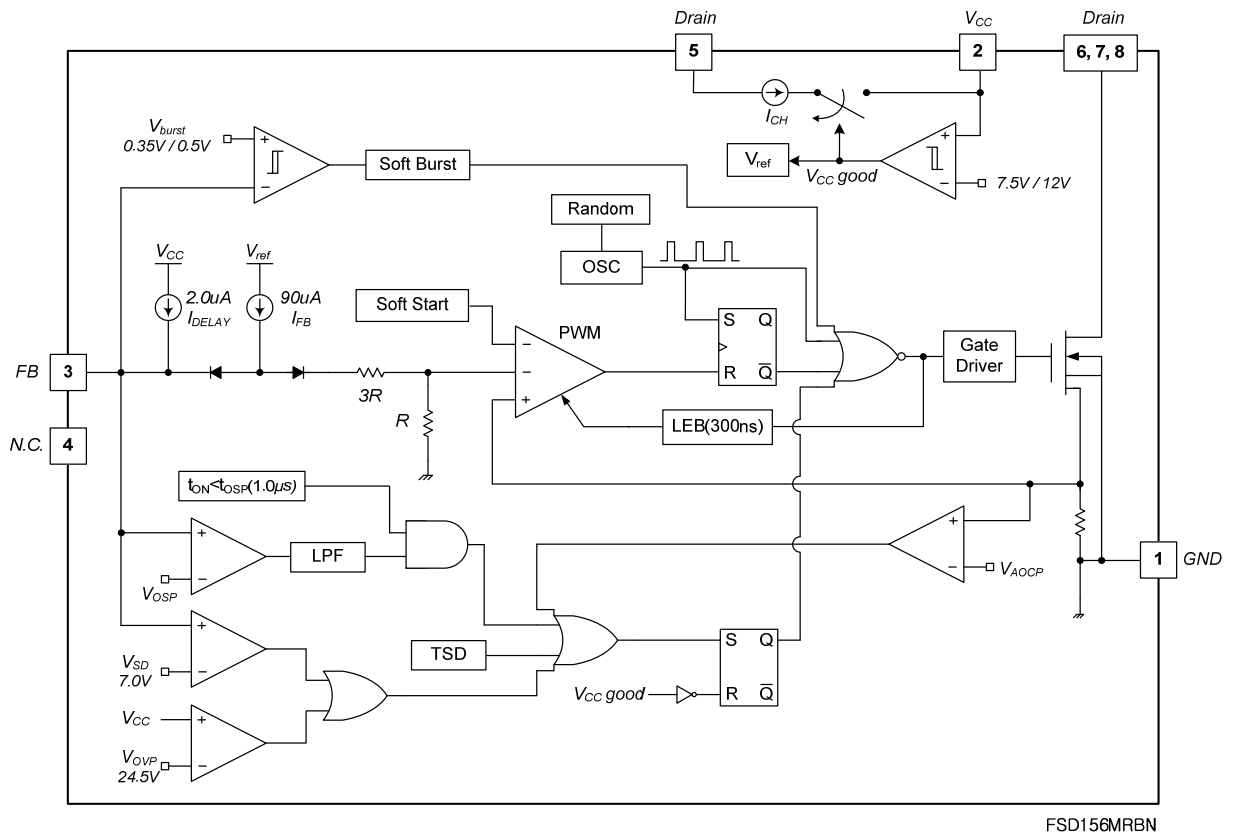


Figure 2. Internal Block Diagram

Pin Configuration

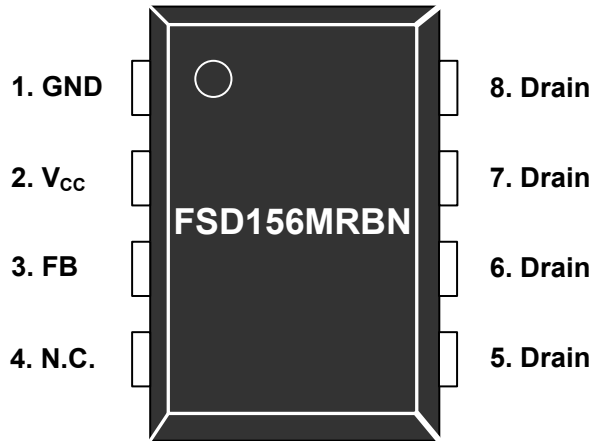


Figure 3. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	GND	Ground. This pin is the control ground and the SenseFET source.
2	V _{CC}	Power Supply. This pin is the positive supply input, which provides the internal operating current for both startup and steady-state operation.
3	FB	Feedback. This pin is internally connected to the inverting input of the PWM comparator. The collector of an opto-coupler is typically tied to this pin. For stable operation, a capacitor should be placed between this pin and GND. If the voltage of this pin reaches 7.0V, the overload protection triggers, which shuts down the FPS™.
4	NC	No Connection
5, 6, 7, 8	Drain	SenseFET Drain. High-voltage power SenseFET drain connection.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V _{DS}	Drain Pin Voltage		650	V
V _{CC}	V _{CC} Pin Voltage		26	V
V _{FB}	Feedback Pin Voltage	-0.3	10.0	V
I _{DM}	Drain Current Pulsed		4	A
I _{DS}	Continuous Switching Drain Current ⁽⁶⁾	T _C =25°C	1.9	A
		T _C =100°C	1.27	A
E _{AS}	Single Pulsed Avalanche Energy ⁽⁷⁾		190	mJ
P _D	Total Power Dissipation (T _C =25°C) ⁽⁸⁾		1.5	W
T _J	Maximum Junction Temperature		150	°C
	Operating Junction Temperature ⁽⁹⁾	-40	+125	°C
T _{STG}	Storage Temperature	-55	+150	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	5	kV
		Charged Device Model, JESD22-C101	2	

Notes:

- Repetitive peak switching current when the inductive load is assumed: Limited by maximum duty (D_{MAX}=0.73) and junction temperature (see Figure 4).
- L=45mH, starting T_J=25°C.
- Infinite cooling condition (refer to the SEMI G30-88).
- Although this parameter guarantees IC operation, it does not guarantee all electrical characteristics.

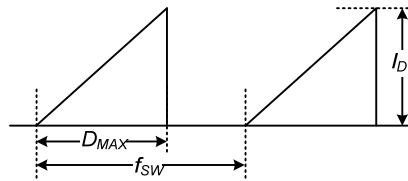


Figure 4. Repetitive Peak Switching Current

Thermal Impedance

T_A=25°C unless otherwise specified.

Symbol	Parameter	Value	Unit
θ _{JA}	Junction-to-Ambient Thermal Impedance ⁽¹⁰⁾	85	°C/W
ψ _{JL}	Junction-to-Lead Thermal Impedance ⁽¹¹⁾	11	°C/W

Notes:

- JEDEC recommended environment, JESD51-2, and test board, JESD51-10, with minimum land pattern.
- Measured on the SOURCE pin #7, close to the plastic interface.

Electrical Characteristics

T_J = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit	
SenseFET Section							
BV _{DSS}	Drain-Source Breakdown Voltage	V _{CC} = 0V, I _D = 250μA	650			V	
I _{DSS}	Zero-Gate-Voltage Drain Current	V _{DS} = 650V, T _A = 25°C			250	μA	
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =10V, I _D =1A		1.8	2.2	Ω	
C _{ISS}	Input Capacitance ⁽¹²⁾	V _{DS} = 25V, V _{GS} = 0V, f=1MHz		515		pF	
C _{OSS}	Output Capacitance ⁽¹²⁾	V _{DS} = 25V, V _{GS} = 0V, f=1MHz		75		pF	
t _r	Rise Time	V _{DS} = 325V, I _D = 4A, R _G =25Ω		26		ns	
t _f	Fall Time	V _{DS} = 325V, I _D = 4A, R _G =25Ω		25		ns	
t _{d(on)}	Turn-On Delay	V _{DS} = 325V, I _D = 4A, R _G =25Ω		14		ns	
t _{d(off)}	Turn-Off Delay	V _{DS} = 325V, I _D = 4A, R _G =25Ω		32		ns	
Control Section							
f _S	Switching Frequency ⁽¹²⁾	V _{CC} = 14V, V _{FB} = 4V	61	67	73	kHz	
Δf _S	Switching Frequency Variation ⁽¹²⁾	-25°C < T _J < 125°C		±5	±10	%	
D _{MAX}	Maximum Duty Ratio	V _{CC} = 14V, V _{FB} = 4V	61	67	73	%	
D _{MIN}	Minimum Duty Ratio	V _{CC} = 14V, V _{FB} = 0V			0	%	
I _{FB}	Feedback Source Current	V _{FB} = 0	65	90	115	μA	
V _{START}	UVLO Threshold Voltage	V _{FB} = 0V, V _{CC} Sweep	11	12	13	V	
V _{STOP}		After Turn-on, V _{FB} = 0V	7.0	7.5	8.0	V	
t _{SS}	Internal Soft-Start Time	V _{STR} = 40V, V _{CC} Sweep		15		ms	
V _{RECOMM}	Recommended V _{CC} Range		13		23	V	
Burst-Mode Section							
V _{BURH}	Burst-Mode Voltage	V _{CC} = 14V, V _{FB} Sweep	0.45	0.50	0.55	V	
V _{BURL}			0.30	0.35	0.40	V	
Hys				150		mV	
Protection Section							
I _{LIM}	Peak Drain Current Limit	di/dt = 300mA/μs	1.45	1.60	1.75	A	
V _{SD}	Shutdown Feedback Voltage	V _{CC} = 14V, V _{FB} Sweep	6.45	7.00	7.55	V	
I _{DELAY}	Shutdown Delay Current	V _{CC} = 14V, V _{FB} = 4V	1.2	2.0	2.8	μA	
t _{LEB}	Leading-Edge Blanking Time ^(12,14)			300		ns	
V _{OVP}	Over-Voltage Protection	V _{CC} Sweep	23.0	24.5	26.0	V	
t _{OSP}	Output-Short Protection ⁽¹²⁾	Threshold Time	OSP Triggered when t _{ON} <t _{OSP} & V _{FB} >V _{OSP} (Lasts Longer than t _{OSP_FB})	0.7	1.0	1.3	μs
V _{OSP}		Threshold V _{FB}		1.8	2.0	2.2	V
t _{OSP_FB}		V _{FB} Blanking Time		2.0	2.5	3.0	μs
TSD	Thermal Shutdown Temperature ⁽¹²⁾	Shutdown Temperature	125	135	145	°C	
T _{HYS}		Hysteresis		60		°C	

Continued on the following page...

Electrical Characteristics (Continued)T_J = 25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device Section						
I _{OP}	Operating Supply Current, (Control Part in Burst Mode)	V _{CC} = 14V, V _{FB} = 0V	0.3	0.4	0.5	mA
I _{OPS}	Operating Switching Current, (Control Part and SenseFET Part)	V _{CC} = 14V, V _{FB} = 2V	1.1	1.5	1.9	mA
I _{START}	Start Current	V _{CC} =11V (Before V _{CC} Reaches V _{START})	85	120	155	μA
I _{CH}	Startup Charging Current	V _{CC} = V _{FB} = 0V, V _{STR} = 40V	0.7	1.0	1.3	mA
V _{STR}	Minimum V _{STR} Supply Voltage	V _{CC} = V _{FB} = 0V, V _{STR} Sweep		26		V

Notes:

12. Although these parameters are guaranteed, they are not 100% tested in production.
13. Average value.
14. t_{LEB} includes gate turn-on time.

Comparison of FSGM300N and FSD156MRBN

Function	FSGM300N	FSD156MRBN	Advantages of FSD156MRBN
Operating Current	1.5mA	0.4mA	Very low standby power
Power Balance	Long t _{CLD}	Very Short t _{CLD}	The difference of input power between the low and high input voltage is quite small.

Typical Performance Characteristics

Characteristic graphs are normalized at $T_A=25^\circ\text{C}$.

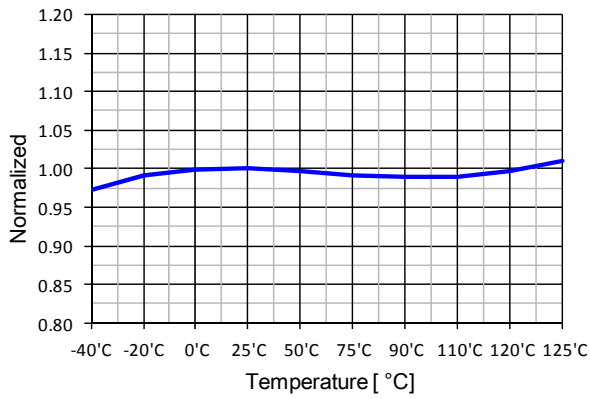


Figure 5. Operating Supply Current (I_{OP}) vs. T_A

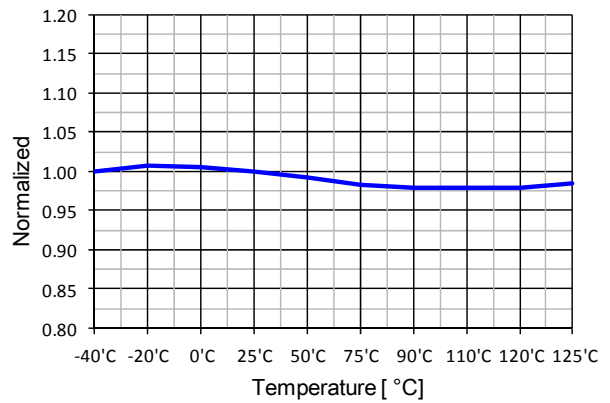


Figure 6. Operating Switching Current (I_{OPS}) vs. T_A

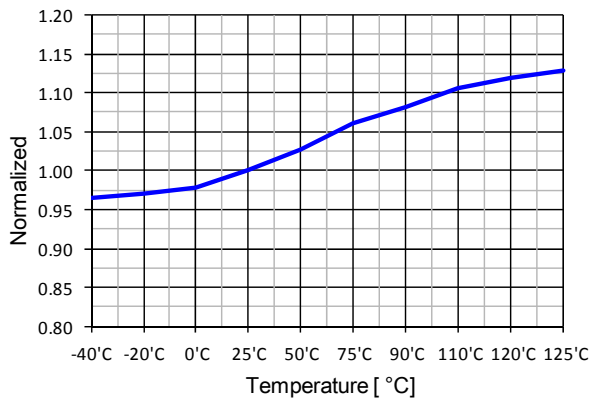


Figure 7. Startup Charging Current (I_{CH}) vs. T_A

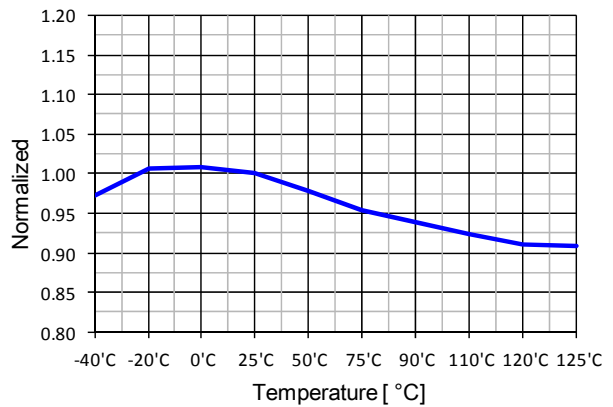


Figure 8. Peak Drain Current Limit (I_{LIM}) vs. T_A

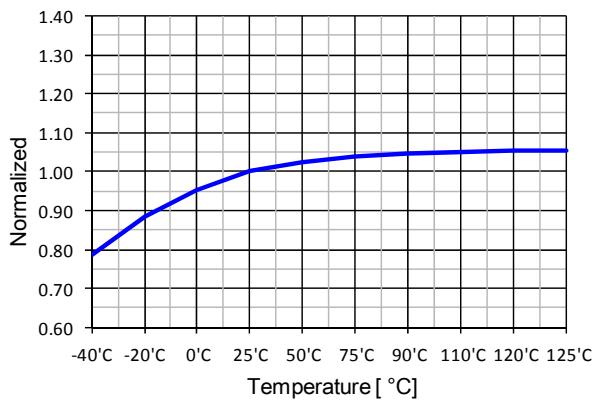


Figure 9. Feedback Source Current (I_{FB}) vs. T_A

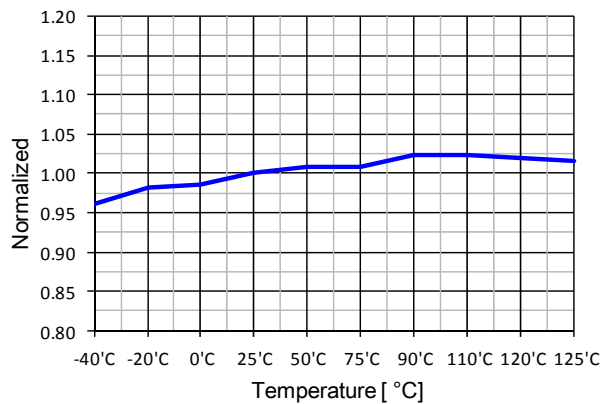


Figure 10. Shutdown Delay Current (I_{DELAY}) vs. T_A

Typical Performance Characteristics

Characteristic graphs are normalized at $T_A=25^\circ\text{C}$.

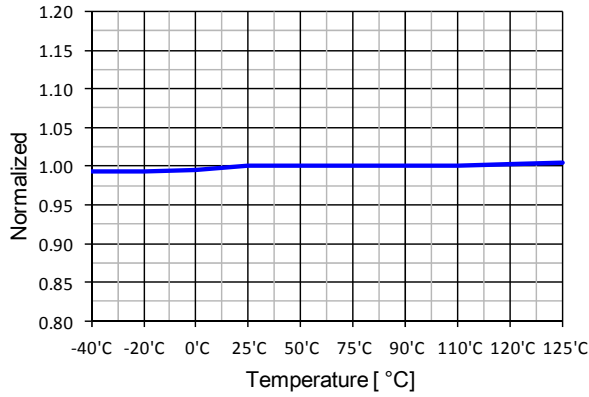


Figure 11. UVLO Threshold Voltage (V_{START}) vs. T_A

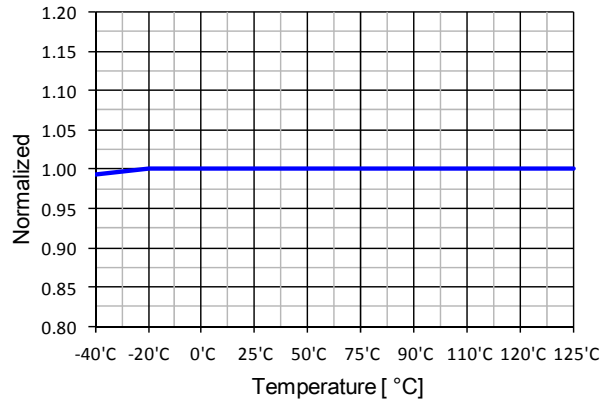


Figure 12. UVLO Threshold Voltage (V_{STOP}) vs. T_A

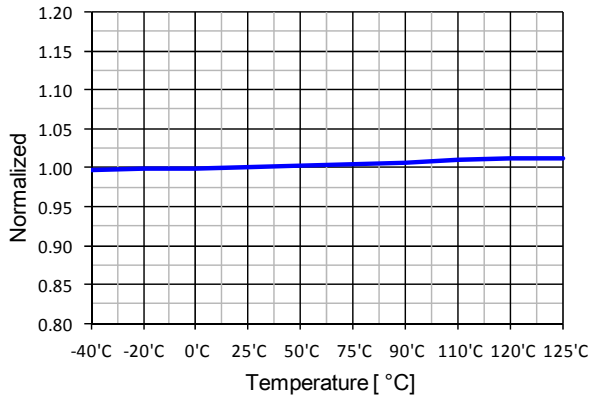


Figure 13. Shutdown Feedback Voltage (V_{SD}) vs. T_A

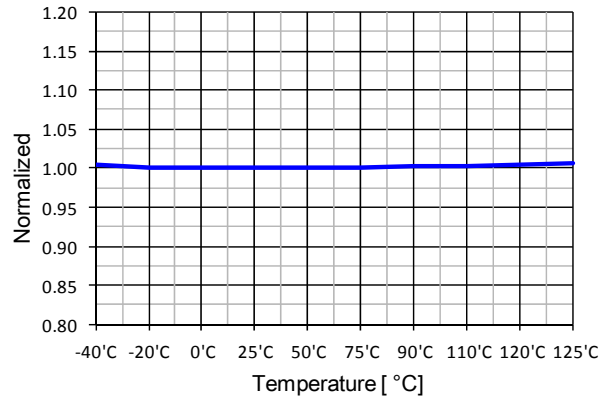


Figure 14. Over-Voltage Protection (V_{OVP}) vs. T_A

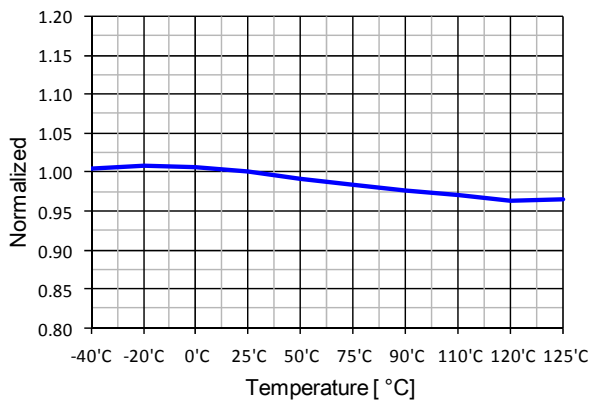


Figure 15. Switching Frequency (f_s) vs. T_A

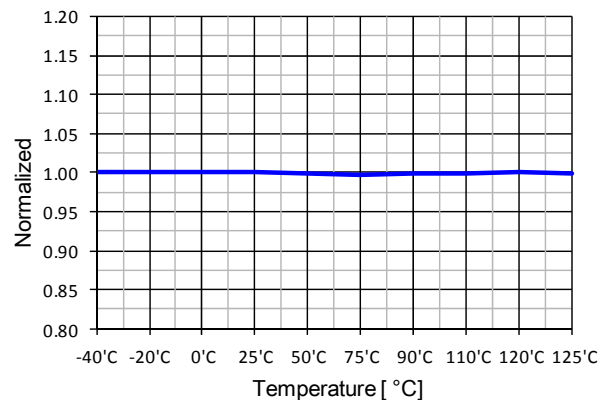


Figure 16. Maximum Duty Ratio (D_{MAX}) vs. T_A

4. Protection Circuits: The FSD156MRBN has several self-protective functions, such as Overload Protection (OLP), Abnormal Over-Current Protection (AOCP), Output-Short Protection (OSP), Over-Voltage Protection (OVP), and Thermal Shutdown (TSD). All the protections are implemented as auto-restart. Once the fault condition is detected, switching is terminated and the SenseFET remains off. This causes V_{CC} to fall. When V_{CC} falls to the Under-Voltage Lockout (UVLO) stop voltage of 7.5V, the protection is reset and the startup circuit charges the V_{CC} capacitor. When V_{CC} reaches the start voltage of 12.0V, the FSD156MRBN resumes normal operation. If the fault condition is not removed, the SenseFET remains off and V_{CC} drops to stop voltage again. In this manner, the auto-restart can alternately enable and disable the switching of the power SenseFET until the fault condition is eliminated. Because these protection circuits are fully integrated into the IC without external components, reliability is improved without increasing cost.

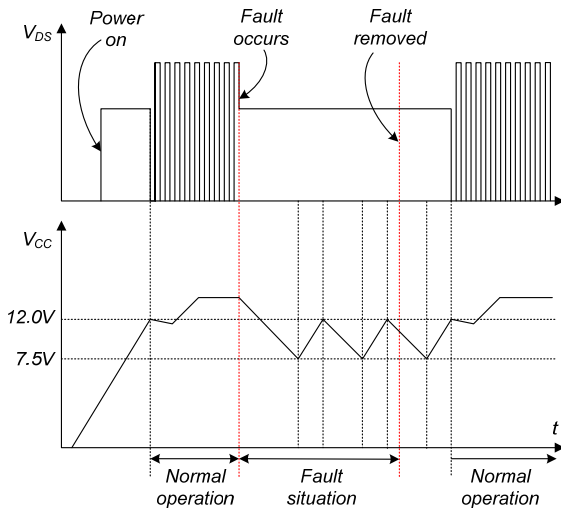


Figure 19. Auto-Restart Protection Waveforms

4.1 Overload Protection (OLP): Overload is defined as the load current exceeding its normal level due to an unexpected abnormal event. In this situation, the protection circuit should trigger to protect the SMPS. However, even when the SMPS is in normal operation, the overload protection circuit can be triggered during the load transition. To avoid this undesired operation, the overload protection circuit is designed to trigger only after a specified time to determine whether it is a transient situation or a true overload situation. Because of the pulse-by-pulse current limit capability, the maximum peak current through the SenseFET is limited and, therefore, the maximum input power is restricted with a given input voltage. If the output consumes more than this maximum power, the output voltage (V_{OUT}) decreases below the set voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, increasing the feedback voltage (V_{FB}). If V_{FB} exceeds 2.5V, D1 is blocked and the 2.0 μ A current source starts to charge C_{FB} slowly up. In this condition, V_{FB} continues

increasing until it reaches 7.0V, when the switching operation is terminated, as shown in Figure 20. The delay for shutdown is the time required to charge C_{FB} from 2.5V to 7.0V with 2.0 μ A. A 25 ~ 50ms delay is typical for most applications. This protection is implemented in Auto-Restart Mode.

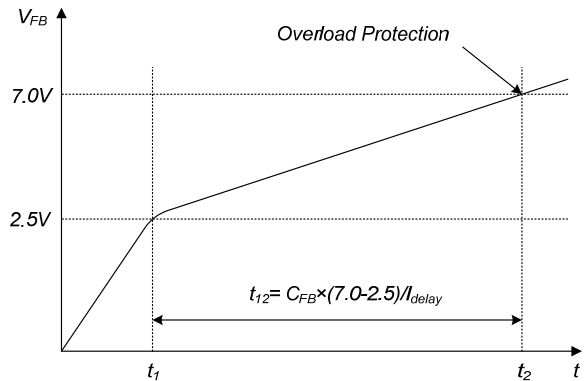


Figure 20. Overload Protection

4.2 Abnormal Over-Current Protection (AOCP): When the secondary rectifier diodes or the transformer pins are shorted, a steep current with extremely high di/dt can flow through the SenseFET during the minimum turn-on time. Even though the FSD156MRBN has overload protection, it is not enough to protect the FSD156MRBN in that abnormal case; due to the severe current stress imposed on the SenseFET until OLP is triggered. The internal AOCP circuit is shown in Figure 21. When the gate turn-on signal is applied to the power SenseFET, the AOCP block is enabled and monitors the current through the sensing resistor. The voltage across the resistor is compared with a preset AOCP level. If the sensing resistor voltage is greater than the AOCP level, the set signal is applied to the S-R latch, resulting in the shutdown of the SMPS.

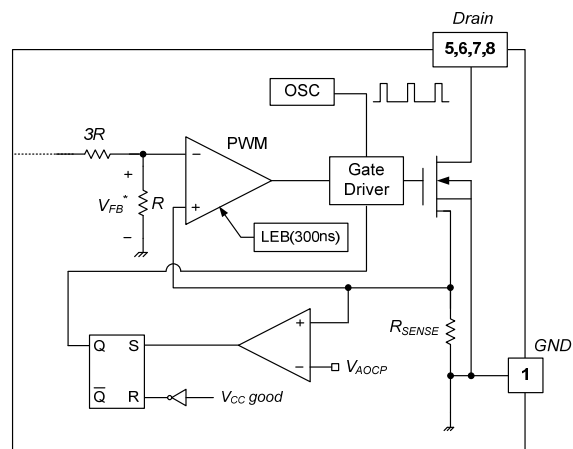


Figure 21. Abnormal Over-Current Protection

4.3. Output-Short Protection (OSP): If the output is shorted, steep current with extremely high di/dt can flow through the SenseFET during the minimum turn-on time. Such a steep current brings high-voltage stress on the drain of the SenseFET when turned off. To protect the device from this abnormal condition, OSP is included. It is comprised of detecting V_{FB} and SenseFET turn-on time. When the V_{FB} is higher than 2.0V and the SenseFET turn-on time is lower than $1.0\mu s$, this condition is recognized as an abnormal error and PWM switching shuts down until V_{CC} reaches V_{START} again. An abnormal condition output short is shown in Figure 22.

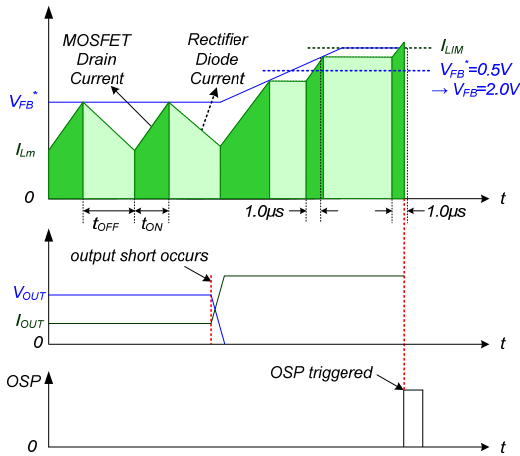


Figure 22. Output-Short Protection

4.4 Over-Voltage Protection (OVP): If the secondary-side feedback circuit malfunctions or a solder defect causes an opening in the feedback path, the current through the opto-coupler transistor becomes almost zero. Then V_{FB} climbs up in a similar manner to the overload situation, forcing the preset maximum current to be supplied to the SMPS until the overload protection is triggered. Because more energy than required is provided to the output, the output voltage may exceed the rated voltage before the overload protection is triggered, resulting in the breakdown of the devices in the secondary side. To prevent this situation, an OVP circuit is employed. In general, the V_{CC} is proportional to the output voltage and the FSD156MRBN uses V_{CC} instead of directly monitoring the output voltage. If V_{CC} exceeds 24.5V, an OVP circuit is triggered, resulting in the termination of the switching operation. To avoid undesired activation of OVP during normal operation, V_{CC} should be designed to be below 24.5V.

4.5 Thermal Shutdown (TSD): The SenseFET and the control IC on a die in one package makes it easier for the control IC to detect the over temperature of the SenseFET. If the temperature exceeds $\sim 135^{\circ}C$, the thermal shutdown is triggered and stops operation. The FSD156MRBN operates in Auto-Restart Mode until the temperature decreases to around $75^{\circ}C$, when normal operation resumes.

5. Soft Burst-Mode Operation: To minimize power dissipation in Standby Mode, the FSD156MRBN enters Burst-Mode operation. As the load decreases, the feedback voltage decreases. As shown in Figure 23, the device automatically enters Burst Mode when the feedback voltage drops below V_{BURL} (350mV). At this point, switching stops and the output voltages start to drop at a rate dependent on standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH} (500mV), switching resumes. The feedback voltage then falls and the process repeats. Burst Mode alternately enables and disables SenseFET switching, reducing switching loss in Standby Mode.

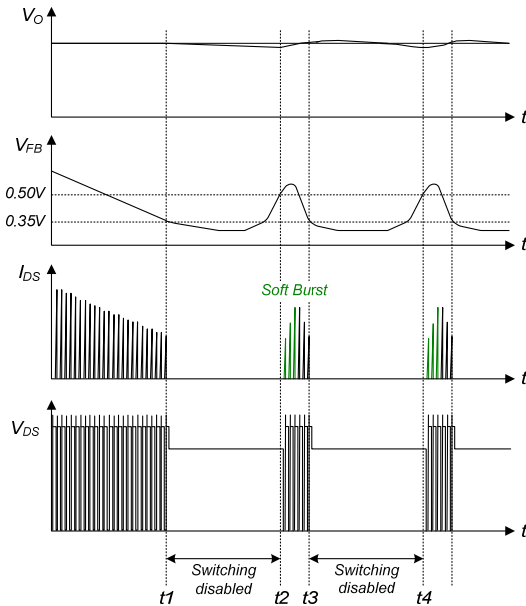


Figure 23. Burst-Mode Operation

6. Random Frequency Fluctuation (RFF): Fluctuating switching frequency of an SMPS can reduce EMI by spreading the energy over a wide frequency range. The amount of EMI reduction is directly related to the switching frequency variation, which is limited internally. The switching frequency is determined randomly by external feedback voltage and internal free-running oscillator at every switching instant. RFF effectively scatters EMI noise around typical switching frequency (67kHz) and can reduce the cost of the input filter included to meet the EMI requirements (e.g. EN55022).

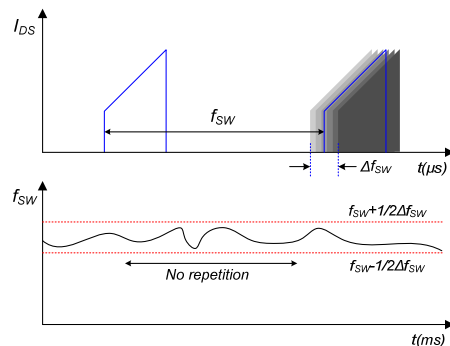


Figure 24. Random Frequency Fluctuation

Typical Application Circuit

Application	Input Voltage	Rated Output	Rated Power
LCD Monitor Power Supply	85 ~ 265V _{AC}	5.0V(2A) 14.0V(1.3A)	28.2W

Key Design Notes

1. The delay for overload protection is designed to be about 30ms with C105 (8.2nF). OLP time between 39ms (12nF) and 46ms (15nF) is recommended.
2. The SMD-type capacitor (C106) must be placed as close as possible to the V_{CC} pin to avoid malfunction by abrupt pulsating noises and to improve ESD and surge immunity. Capacitance between 100nF and 220nF is recommended.

Schematic

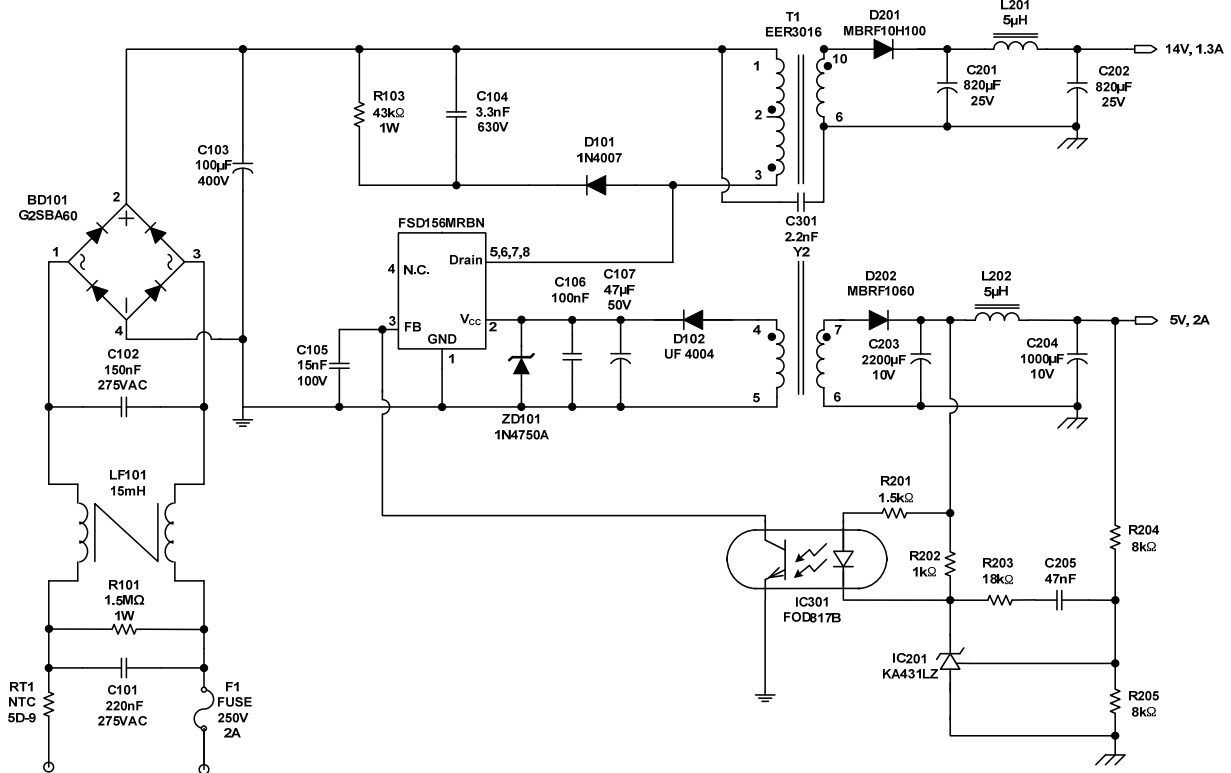


Figure 25. Schematic

Transformer

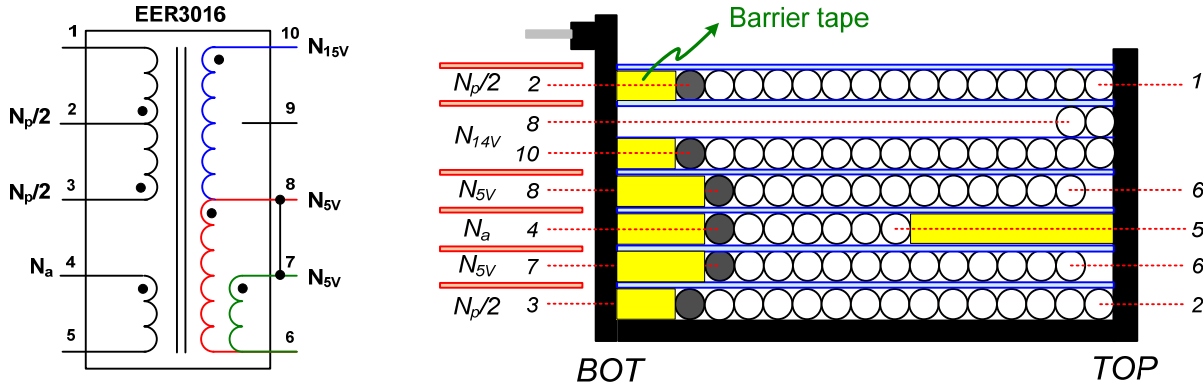


Figure 26. Schematic of Transformer

Winding Specification

	Pin(S → F)	Wire	Turns	Winding Method	Barrier Tape		
					TOP	BOT	Ts
$N_p/2$	3 → 2	0.25φ×1	22	Solenoid Winding	-	2.0mm	1
Insulation: Polyester Tape t = 0.025mm, 2 Layers							
N_{5V}	7 → 6	0.4φ×2 (TIW)	3	Solenoid Winding	-	3.0mm	1
Insulation: Polyester Tape t = 0.025mm, 2 Layers							
N_a	4 → 5	0.2φ×1	8	Solenoid Winding	4.0mm	3.0mm	1
Insulation: Polyester Tape t = 0.025mm, 2 Layers							
N_{5V}	8 → 6	0.4φ×2 (TIW)	3	Solenoid Winding	-	3.0mm	1
Insulation: Polyester Tape t = 0.025mm, 2 Layers							
N_{14V}	10 → 8	0.4φ×2 (TIW)	5	Solenoid Winding	-	2.0mm	1
Insulation: Polyester Tape t = 0.025mm, 2 Layers							
$N_p/2$	2 → 1	0.25φ×1	22	Solenoid Winding	-	2.0mm	1
Insulation: Polyester Tape t = 0.025mm, 2 Layers							

Electrical Characteristics

	Pin	Specification	Remark
Inductance	1–3	826μH ±6%	67kHz, 1V
Leakage	1–3	15μH Maximum	Short all other pins

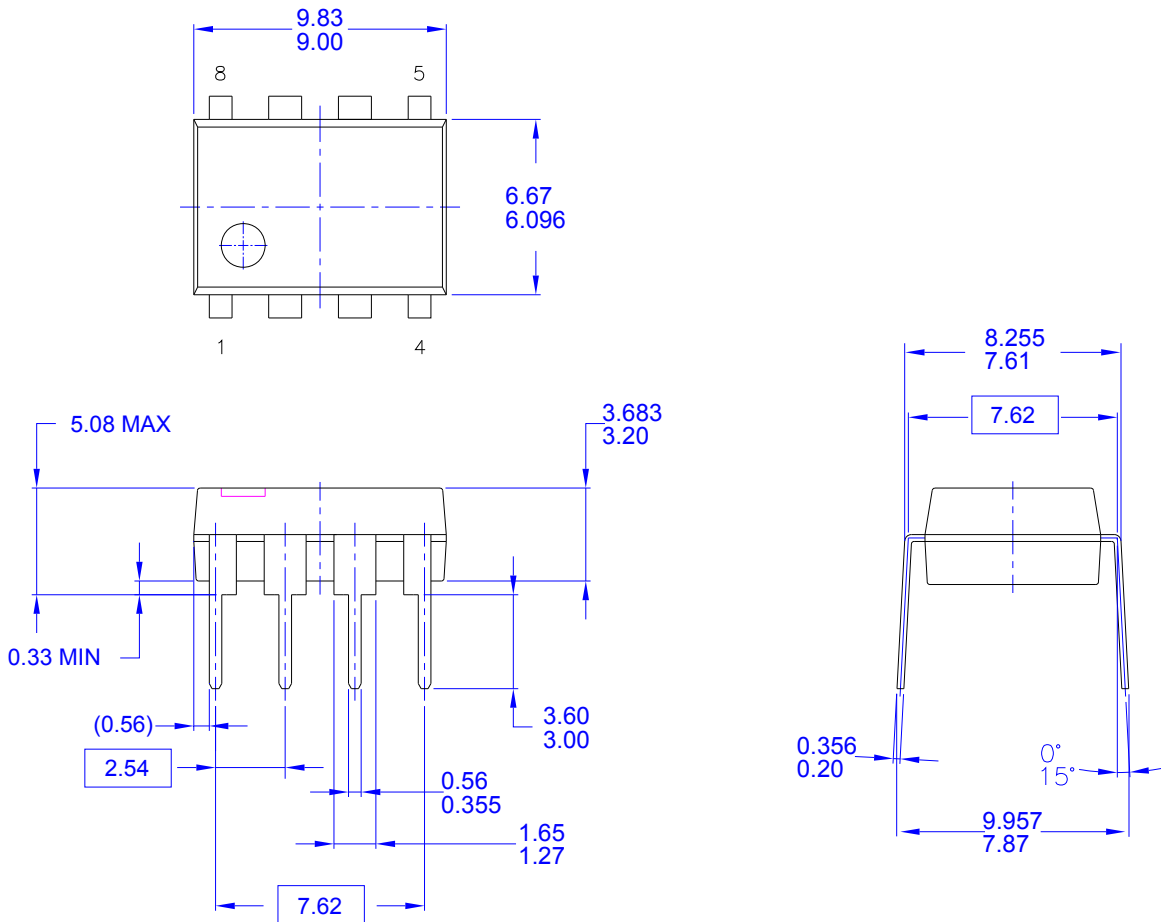
Core & Bobbin

- Core: EER3016 ($A_e=109.7\text{mm}^2$)
- Bobbin: EER3016

Bill of Materials

Part #	Value	Note	Part #	Value	Note
Fuse			Capacitor		
F101	250V 2A		C101	220nF/275V	Box (Pilkor)
NTC			C102	150nF/275V	Box (Pilkor)
NTC101	5D-9	DSC	C103	100 μ F/400V	Electrolytic (SamYoung)
Resistor			C104	3.3nF/630V	Film (Sehwa)
R101	1.5M Ω , J	1W	C105	15nF/100V	Film (Sehwa)
R103	43k Ω , J	1W	C106	100nF	SMD (2012)
R201	1.5k Ω , F	1/4W, 1%	C107	47 μ F/50V	Electrolytic (SamYoung)
R202	1.0k Ω , F	1/4W, 1%	C201	820 μ F/25V	Electrolytic (SamYoung)
R203	18k Ω , F	1/4W, 1%	C202	820 μ F/25V	Electrolytic (SamYoung)
R204	8k Ω , F	1/4W, 1%	C203	2200 μ F/10V	Electrolytic (SamYoung)
R205	8k Ω , F	1/4W, 1%	C204	1000 μ F/16V	Electrolytic (SamYoung)
			C205	47nF/100V	Film (Sehwa)
			C301	2.2nF/Y2	Y-cap (Samhwa)
IC			Inductor		
FPS	FSD156MRBN	Fairchild	LF101	20mH	Line filter 0.5 \emptyset
IC201	KA431LZ	Fairchild	L201	5 μ H	5A Rating
IC301	FOD817B	Fairchild	L202	5 μ H	5A Rating
Diode			Transformer		
D101	1N4007	Vishay	T101	826 μ H	
D102	UF4007	Vishay			
ZD101	1N4750	Vishay			
D201	MBRF10H100	Fairchild			
D202	MBRF1060	Fairchild			
BD101	G2SBA60	Vishay			

Package Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MS-001 VARIATION BA
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D) DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994
- E) DRAWING FILENAME AND REVISION: MKT-N08FREV2.

Figure 27. 8-Lead, MDIP, JEDEC MS-001, .300" Wide






Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
<http://www.fairchildsemi.com/packaging/>.



TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

- | | | | |
|--|---|---|---|
| 2Cool™ | FPST™ | PDP SPM™ | The Power Franchise® |
| AccuPower™ | F-PFS™ | Power-SPM™ | the power franchise |
| Auto-SPM™ | FRFET® | PowerTrench® | TinyBoost™ |
| AX-CAP™ | Global Power Resource SM | PowerXS™ | TinyBuck™ |
| BitSiC™ | Green FPS™ | Programmable Active Droop™ | TinyCalc™ |
| Build it Now™ | Green FPS™ e-Series™ | QFET® | TinyLogic® |
| CorePLUS™ | Gmax™ | QST™ | TINYOPTO™ |
| CorePOWER™ | GTO™ | Quiet Series™ | TinyPower™ |
| CROSSVOL7™ | IntelliMAX™ | Rapid Configure™ | TinyPWM™ |
| CTL™ | ISOPLANAR™ |  ™ | TinyWire™ |
| Current Transfer Logic™ | Making Small Speakers Sound Louder and Better™ | Saving our world, 1mW/WkV at a time™ | TranSiC™ |
| DEUXPEED® | MegaBuck™ | SignalWise™ | TriFault Detect™ |
| Dual Cool™ | MICROCOUPLER™ | SmartMax™ | TRUECURRENT® |
| EcoSPARK® | MicroFET™ | SMART START™ | μSerDes™ |
| EfficientMax™ | MicroPak™ | Solutions for Your Success™ |  ™ |
| ESBC™ | MicroPak2™ | SPM® | UHC® |
|  Fairchild® | MillerDrive™ | STEALTH™ | Ultra FRFET™ |
| Fairchild Semiconductor® | MotionMax™ | SuperFET® | UniFET™ |
| FACT Quiet Series™ | Motion-SPM™ | SuperSOT™.3 | VCX™ |
| FACT® | mWSaver™ | SuperSOT™.6 | VisualMax™ |
| FAST® | OptoHiT™ | SuperSOT™.8 | VoltagePlus™ |
| FastvCore™ | OPTOLOGIC® | SupreMOS® | XS™ |
| FETBench™ | OPTOPLANAR® | SyncFET™ | |
| FlashWriter® |  ™ | Sync-Lock™ | |
| | |  ™ | |

* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. 158